5539 89742

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 3-24-03 Serial # 09/987,607 Priority Application Date 1-17-95

Your Name David Hogans Examiner # 79069

AU 2813 Phone 305-3361 Room CP4-4D14

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

03-24-03 P03:35 IN

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: (USPT) (DWPI) (EPO Abs) (JPO Abs) IBM TDB
Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. 5,612,254 to Hu et al. ; 5,504,029 to Murata et al. ; Re 33,829 to Castleberry

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ✓ Other _____
Secondary Refs ✓ Foreign Patents ✓
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

liquid crystal or LCD ; active matrix ; multilevel or multilayer; insulator or dielectric ; silicon nitride (SiN) + silicon dioxide (SiO_2) ; gate electrode ; interlayer w/ at least 2 layers (SiN + SiO_2) ; pixel electrode ; source or drain electrode ; source or drain electrode contacts pixel electrode ; etching to form contacts /open#3/ via /holes ; etch selectivity or different etch characteristics ; etch stopper

Staff Use Only
Searcher: Derrick Blalock
Searcher Phone: 306-0936
Searcher Location: STIC-EIC2800, CP4-9C18.
Date Searcher Picked Up: 3/24/03
Date Completed: 3/25/03
Searcher Prep/Rev Time: _____
Online Time: _____

Type of Search
Structure (#)_____
Bibliographic ✓
Litigation_____
Fulltext_____
Patent Family_____
Other_____

Vendors
STN ✓
Dialog ✓
Questel/Orbit_____
Lexis-Nexis_____
WWW/Internet_____
Other _____

03/25/03

Re: 09/987,607

Examiner Hogans

Attached are edited search results from the patent and nonpatent databases.

Red tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Derrick Blalock,
STIC-EIC2800
306-0935
CP4-9C18

03/25/2003

SYSTEM:OS - DIALOG OneSearch
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03/25/2003

Set	Items	Description
S1	150507	LCD OR LC(W)DISPLAY? OR LIQUID(W)CRYSTAL OR CC=(B4150D OR B7260)
S2	1308996	MATRIX OR MATRICES OR MATRIXES
S3	310478	(MULTILEVEL OR MULTI(W)LEVEL OR MULTILAYER? OR MULTI(W)LAYER)
S4	395594	MULTILEVEL OR MULTI(W)LEVEL OR MULTILAYER? OR MULTI(W)LAYER OR BILAYER? OR BI(W)LAYER? OR TRI(W)LAYER? OR TRILAYER?
S5	965601	INSULAT? OR DIELECTRIC
S6	124150	(SILICON)(W)(NITRIDE OR MONONITRIDE) OR SIN OR SI(W)N
S7	2976	CI=(SI SS(S)N SS)(S)NE=2
S8	562510	(SILICON)(W)(DIOXIDE OR MONOOXIDE) OR SIO OR SI(W)O OR SILICON(W)OXIDE OR SILICA OR SIO2 OR SI(W)O2
S9	7397	CI=(SI SS(S)O SS)(S)NE=2
S10	5837	GATE(W)ELECTRODE? ?
S11	309	PIXEL(W)ELECTRODE? ?
S12	2420	(SOURCE OR DRAIN)(2N)(ELECTRODE? ?)
S13	3531213	CONTACT? ? OR OPEN? OR VIA OR HOLE? ?
S14	229306	ETCH???
S15	7	S1 AND S7 AND S9
S16	77	S1 AND S6 AND S8
S17	7	S15
S18	7	RD (unique items)
S19	77	S16
S20	74	S19 NOT S15
S21	56	RD (unique items)
S22	9	S21 AND S2
S23	3	S21 AND S10
S24	0	S21 AND S11
S25	1	S21 AND S12
S26	34	S21 AND S5
S27	5	S21 AND S3
S28	26215	S2 AND S5
S29	959	S28 AND S1
S30	59	S29 AND (S6 OR S7)
S31	61	S29 AND (S8 OR S9)
S32	36	S22:S27
S33	20	S21 NOT S32
S34	51	S30 NOT S21
S35	34	RD (unique items)
S36	49	S31 NOT (S30 OR S21)
S37	46	RD (unique items)
S38	5041	AU=(ZHANG, HONGYONG OR ZHANG HONGYONG OR ZHANG, H OR ZHANG H)
S39	31	S38 AND S1
S40	0	S39 AND (S6 OR S7)
S41	2	S39 AND (S8 OR S9)

18/3,AB,CI/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5468869 INSPEC Abstract Number: B9702-4260-005
Title: Thickness effects of SiO/sub x/N/sub y/ interlayer inserted between BaTiO/sub 3/ insulating layer and ZnS:Mn phosphor layer in thin film electroluminescent devices
Author(s): Song, M.H.; Lee, Y.H.; Hahn, T.S.; Oh, M.H.; Yoon, K.H.
Author Affiliation: Div. of Electron. & Inf., Korea Inst. of Sci. & Technol., Seoul, South Korea
Journal: Journal of Crystal Growth vol.167, no.1-2 p.157-64
Publisher: Elsevier,
Publication Date: Sept. 1996 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199609)167:1/2L.157:TESI;1-7
Material Identity Number: J037-96020
U.S. Copyright Clearance Center Code: 0022-0248/96/$15.00
Language: English
Abstract: We investigated the effects of a SiO/sub x/N/sub y/ interlayer on a thin film electroluminescent device, inserted between an amorphous BaTiO/sub 3/ thin film and a ZnS:Mn phosphor layer. The effects on the thin film electroluminescent device was studied as a function of the thickness of the interlayer. We found that the introduction of the interlayer affected the growth behavior of the phosphor layer. With increasing thickness of the interlayer, the average grain size and the crystallinity of the phosphor layer was improved. The turn-on voltage of the electroluminescent device increased, and the saturation brightness slightly decreased with increasing interlayer thickness. In the case of the TFELD without the interlayer, Poole-Frenkel conduction was observed in the low dc field region, the devices with the interlayer exhibited effective electron tunneling from interface traps. The efficiency of the devices increased with increasing interlayer thickness.
Subfile: B
Chemical Indexing:
BaTiO3-SiON-ZnS:Mn int - BaTiO3 int - ZnS:Mn int - SiON int - TiO3 int - ZnS int - Ba int - Mn int - O3 int - Si int - Ti int - Zn int - N int - O int - S int - BaTiO3 ss - ZnS:Mn ss - SiON ss - TiO3 ss - Ba ss - Mn ss - O3 ss - **Si ss** - Ti ss - Zn ss - **N ss** - **O ss** - S ss - ZnS bin - Zn bin - S bin - Mn el - Mn dop (Elements - 3,3,**2**,1,3,8)

18/3,AB,CI/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5237029 INSPEC Abstract Number: B9605-4270-021
Title: Fabrication of amorphous silicon alloy optical devices for new type of thin film optoelectronic integrated circuits
Author(s): Kruangam, D.; Boonkosum, W.; Ratwises, B.; Sujaridchai, T.; Panyakeow, S.
Author Affiliation: Semicond. Device Res. Lab., Chulalongkorn Univ., Bangkok, Thailand
Conference Title: 13th Australian Microelectronics Conference. Microelectronics: Technology Today for the Future. Proceedings. MICRO `95 p.259-64
Publisher: IREE Soc, Milsons Point, NSW, Australia
Publication Date: 1995 Country of Publication: Australia xii+333 pp.
ISBN: 0 909394 38 5 Material Identity Number: XX95-01929

Conference Title: Proceeding of Microelectronics 1995. MICRO`95
Conference Date: 16-19 July 1995 Conference Location: Adelaide, SA, Australia
Language: English
Abstract: Integrated type amorphous silicon alloy thin film light emitting diodes (TFLEDs) have been fabricated for the first time. It is demonstrated that a new type of low cost flat panel display and thin film photocoupler can be realized by using the amorphous TFLEDs as light sources. The devices can be operated at modulation frequencies as high as several hundred kHz.
Subfile: B
Chemical Indexing:
Si:H int - Si int - H int - Si:H bin - Si bin - H bin - Si el - H el - H dop (Elements - 1,1,2)
SiC:H int - SiC int - Si int - C int - H int - SiC:H ss - Si ss - C ss - H ss - SiC bin - Si bin - C bin - H el - H dop (Elements - 2,1,3)
SiN:H int - SiN int - Si int - H int - N int - SiN:H ss - **Si ss** - H ss - **N ss** - SiN bin - Si bin - N bin - H el - H dop (Elements - **2**,1,3)
SiO2:H int - SiO2 int - O2 int - Si int - H int - O int - SiO2:H ss - SiO2 ss - O2 ss - **Si ss** - H ss - **O ss** - SiO2 bin - O2 bin - Si bin - O bin - H el - H dop (Elements - **2**,1,3)

18/3,AB,CI/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5100706 INSPEC Abstract Number: B9512-7260-028
Title: Novel thin film light emitting diode display made of amorphous silicon-based semiconductors
Author(s): Kruangam, D.; Boonkosum, W.; Panyakeow, S.; DeLong, B.
Author Affiliation: Semicond. Device Res. Lab., Chulalongkorn Univ., Bankok, Thailand
Conference Title: Flat Panel Display Materials. Symposium p.305-10
Editor(s): Batey, J.; Chiang, A.; Holloway, P.H.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA ix+339 pp.
Conference Title: Flat Panel Display Materials. Symposium
Conference Date: 5-6 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: A novel thin film light emitting diode (TFLED) flat panel display was developed. The TFLED is a carrier injection-type electroluminescent device and is made from hydrogenated amorphous silicon-based semiconductor p-i-n junctions. The amorphous layers employed in this work are, for example, a-Si/sub 1-x/C/sub x/:H and a-Si/sub 1-x/N/sub x/:H. The TFLED has two basic structures: (1) glass substrate/ITO/amorphous p-i-n layers/Al and (2) metal sheet substrate/amorphous n-i-p layers/ITO. The typical thicknesses of the amorphous p-i-n layers are 150 AA, 500 AA and 500 AA, respectively. The color of the emission can be changed from red to white-blue by increasing the optical energy gap (2.5-3.5 eV), i.e. the atomic fraction x, in the i-layer. The brightness of the TFLEDs is of the order of 1-10 cd/m/sup 2/ with injection current density of 100-1000 mA/cm/sup 2/ and applied voltage of 8-15 V.
Subfile: B
Chemical Indexing:
Al-SiC:H-InSnO int - InSnO int - SiC:H int - SiC int - Al int - In int - Si int - Sn int - C int - H int - O int - InSnO ss - SiC:H ss - In ss -

Si ss - Sn ss - C ss - H ss - **O ss** - SiC bin - Si bin - C bin - Al el - H el - H dop (Elements - 1,**2**,1,3,3,7)
Al-SiN:H-InSnO int - InSnO int - SiN:H int - SiN int - Al int - In int - Si int - Sn int - H int - N int - O int - InSnO ss - SiN:H ss - In ss - **Si ss** - Sn ss - H ss - **N ss** - **O ss** - SiN bin - Si bin - N bin - Al el - H el - H dop (Elements - 1,**2**,1,3,3,7)
SiC:H-InSnO int - InSnO int - SiC:H int - SiC int - In int - Si int - Sn int - C int - H int - O int - InSnO ss - SiC:H ss - In ss - **Si ss** - Sn ss - C ss - H ss - **O ss** - SiC bin - Si bin - C bin - H el - H dop (Elements - **2**,1,3,3,6)
SiN:H-InSnO int - InSnO int - SiN:H int - SiN int - In int - Si int - Sn int - H int - N int - O int - InSnO ss - SiN:H ss - In ss - **Si ss** - Sn ss - H ss - **N ss** - **O ss** - SiN bin - Si bin - N bin - H el - H dop (Elements - **2**,1,3,3,6)

18/3,AB,CI/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5100667 INSPEC Abstract Number: B9512-2560R-049
Title: Effects of N/sub 2/ plasma treatment on SiO/sub 2/ gate insulator in a-Si:H thin film transistor
Author(s): Sung Chul Kim; Sung Sig Bae; Eui Yeol Oh; Jeong Hyun Kim; Jong Wan Lee; Cha Yeon Kim; Donggil Kim
Author Affiliation: GoldStar Co. Ltd., Kyongki-do, South Korea
Conference Title: Flat Panel Display Materials. Symposium p.29-34
Editor(s): Batey, J.; Chiang, A.; Holloway, P.H.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA ix+339 pp.
Conference Title: Flat Panel Display Materials. Symposium
Conference Date: 5-6 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: We fabricated a high performance a-Si:H TFT using N/sub 2/ plasma treated APCVD SiO/sub 2/ as a gate insulator. The effects of N/sub 2/ plasma treatment on the APCVD SiO/sub 2/ were investigated by XPS and SIMS measurements, and the formation of an oxynitride interface layer between a-Si:H and APCVD SiO/sub 2/ was found in the a-Si:H TFT. From our experimental results, it may be concluded that most nitrogen atoms, which were incorporated by the exposure of the SiO/sub 2/ layer to the N/sub 2/ plasma, exist without bonds to other atoms near the surface of the SiO/sub 2/ layer. During the sequential deposition of a-Si:H on the N/sub 2/ plasma treated APCVD SiO/sub 2/ layer, Si-N bonds are formed, resulting in the oxynitride layer in the interface region. This explains the high performance of the a-Si:H TFT with the N/sub 2/ plasma treated APCVD SiO/sub 2/ gate insulator.
Subfile: B
Chemical Indexing:
AlCr-Si:H-SiON-SiO2-Cr int - AlCr int - Si:H int - SiO2 int - SiON int - Al int - Cr int - O2 int - Si int - H int - N int - O int - SiON ss - **Si ss** - **N ss** - **O ss** - AlCr bin - Si:H bin - SiO2 bin - Al bin - Cr bin - O2 bin - Si bin - H bin - O bin - Cr el - Si el - H el - H dop (Elements - **2**,1,1,**2**,3,**2**,1,6)

18/3,AB,CI/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

03651566 INSPEC Abstract Number: B90044017
Title: Amorphous silicon thin-film transistors with SiO/sub x/N/sub y//SiN/sub x/ gate insulators
Author(s): Hiranaka, K.; Yamaguchi, T.
Author Affiliation: Fujitsu Labs. Ltd., Atsugi, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.29, no.2 p.229-35
Publication Date: Feb. 1990 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
Language: English
Abstract: A double layer of plasma chemical vapor deposition SiO/sub x/N/sub y/ and SiN/sub x/ was applied to the gate insulator of an amorphous silicon (a-Si) thin-film transistor (TFT). When a thin SiN/sub x/ layer is inserted between the a-Si of an a-Si TFT and the SiO/sub x/N/sub y/ gate insulator, the density of trapped charges is found to decrease less than for a gate insulator with only SiN/sub x/, when the thickness of SiN/sub x/ is decreased. No deterioration was observed in the switching characteristics of an a-Si TFT with a SiO/sub x/N/sub y//SiN/sub x/ gate insulator, compared with a-Si TFTs with SiN/sub x/ gate insulators commonly used in **liquid crystal** displays. The density of trapped charges is related to the threshold voltage shift.
Subfile: B
Chemical Indexing:
Si-SiON-SiN int - SiON int - SiN int - Si int - N int - O int - SiON ss - **Si ss** - **N ss** - **O ss** - SiN bin - Si bin - N bin - Si el (Elements - 1,3,**2**,3)

18/3,AB,CI/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03463849 INSPEC Abstract Number: B89065268
Title: Improved stability of ZnS:Mn ACTFEL devices
Author(s): Khormaei, R.; Wager, J.F.; King, C.N.
Author Affiliation: Oregon State Univ., Corvallis, OR, USA
Conference Title: 1989 SID International Symposium. Digest of Technical Papers p.65-7
Editor(s): Morreale, J.
Publisher: Soc. Inf. Display, Playa del Ray, CA, USA
Publication Date: 1989 Country of Publication: USA x+440 pp.
Conference Date: 16-18 May 1989 Conference Location: Baltimore, MD, USA
Language: English
Abstract: Several approaches have been employed to reduce brightness-voltage instabilities of ZnS:Mn ACTFEL displays. One approach involves the addition of a CaS layer at one or both of the phosphor/insulator interfaces. Another approach involves oxygen exposure of ZnS prior to second insulator deposition. Major improvements are observed, as determined by brightness-voltage aging and latent image experiments.
Subfile: B
Chemical Indexing:
SiON-CaS-ZnS:Mn int - ZnS:Mn int - SiON int - CaS int - ZnS int - Ca int - Mn int - Si int - Zn int - N int - O int - S int - ZnS:Mn ss - SiON ss - Mn ss - **Si ss** - Zn ss - **N ss** - **O ss** - S ss - CaS bin - ZnS bin - Ca bin - Zn bin - S bin - Mn el - Mn dop (Elements - 3,**2**, **2**,1,3,7)

18/3,AB,CI/7 (Item 7 from file: 2)

03/25/2003

DIALOG(R)File 2:INSPEC

03338311 INSPEC Abstract Number: B89026546
Title: Dielectrics for bright EL displays
Author(s): Tiku, S.K.; Rustomji, S.H.
Author Affiliation: Sigmatron Nova Inc., Thousand Oaks, CA, USA
Conference Title: Conference Record of the 1988 International Display Research Conference (IEEE Cat. No.88-CH-2678-1) p.36-41
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA 240 pp.
U.S. Copyright Clearance Center Code: CH2678-1/88/0000-0036$01.00
Conference Sponsor: IEEE; Soc. Inf. Display; Advisory Group on Electron Devices
Conference Date: 4-6 Oct. 1988 Conference Location: San Diego, CA, USA
Language: English
Abstract: Thin-film electroluminescence as a practical flat-panel technology is considered. It is shown that stacked dielectrics, which are more amenable to high-volume production than composite dielectrics, can give dielectric layers with high figures of merit and can be utilized to maximize the dielectric capacitance and the phosphor thickness. However, the fraction of the applied voltage that is applied across the ZnS layer must be limited to about 70%. Because of the nature of the breakdown mechanism in Ta/sub 2/O/sub 5/ and its adhesion properties, the use of this material must be limited, and its placement in the stack carefully chosen. Ta/sub 2/O/sub 5/ should not be sputter-deposited on top of ITO or ZnS and its contact with aluminum should be preferably avoided. Extra brightness improvements must come from the phosphor process. High brightness and efficiencies have been attained in the SiON/Ta/sub 2/O/sub 5/ (ST) and Al/sub 2/O/sub 3//Ta/sub 2/O/sub 5/ (AT) stacked dielectric systems. The ST system is preferable because of its tolerance to subsequent processing steps.
Subfile: B
Chemical Indexing:
Al2O3-Ta2O5 int - Al2O3 int - Ta2O5 int - Al2 int - Ta2 int - Al int - O3 int - O5 int - Ta int - O int - Al2O3 bin - Ta2O5 bin - Al2 bin - Ta2 bin - Al bin - O3 bin - O5 bin - Ta bin - O bin (Elements - 2,2,3)
SiON-Ta2O5 int - Ta2O5 int - SiON int - Ta2 int - O5 int - Si int - Ta int - N int - O int - SiON ss - **Si ss - N ss - O ss** - Ta2O5 bin - Ta2 bin - O5 bin - Ta bin - O bin (Elements - 3,**2**,4)
ZnS int - Zn int - S int - ZnS bin - Zn bin - S bin (Elements - 2)

32/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7122044 INSPEC Abstract Number: B2002-01-2560R-082
Title: A self-passivated Cu(Mg) **gate electrode** for an amorphous silicon thin-film transistor
Author(s): Lee, W.H.; Cho, B.S.; Kang, B.J.; Yang, H.J.; Lee, J.G.; Woo, I.K.; Lee, S.W.; Jang, J.; Chae, G.S.; Soh, H.S.
Author Affiliation: Sch. of Metall. & Mater. Eng., Kookmin Univ., Seoul, South Korea
Journal: Applied Physics Letters vol.79, no.24 p.3962-4
Publisher: AIP,
Publication Date: 10 Dec. 2001 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(20011210)79:24L.3962:SPGE;1-7
Material Identity Number: A135-2001-050
U.S. Copyright Clearance Center Code: 0003-6951/2001/79(24)/3962(3)/$18.00
Language: English
Abstract: The feasibility of using Cu(Mg) alloy film as a **gate electrode** for thin-film transistor (TFT) **liquid crystal** displays has been investigated. When pure Cu was used as a **gate electrode**, severe interdiffusion occurred between Cu and the gases SiH/sub 4/, NH/sub 3/, and CF/sub 4/ during plasma-enhanced chemical vapor deposition of a gate **dielectric**, **SiN**/sub x/, and dry etching of the **SiN** /sub x/. On the other hand, the deposition of a Cu(Mg) alloy film gives rise to the formation of a MgO/Cu bilayer structure with low Cu resistivity, good adhesion to **SiO** /sub 2/, higher leakage current density, and excellent passivation capability. A hydrogenated amorphous silicon TFT with a MgO encapsulated Cu gate exhibited a gate voltage swing of 0.91 V/dec. and a threshold voltage of 6.8 V, resulting in a reduction of process steps and better performance.
Subfile: B

32/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6990728 INSPEC Abstract Number: B2001-09-7260D-023
Title: Back-channel effects on the threshold voltage of low-temperature poly-Si TFTs with **SiN**/sub x//**SiO**/sub 2/ dual under layer
Author(s): Kawamura, S.; Nishibe, T.; Ibaraki, N.; Hiramatsu, M.
Author Affiliation: Toshiba LCD R&D Center, Saitama, Japan
Conference Title: Society for Information Display 1999 International Symposium p.456-9
Publisher: Soc. Inf. Display (SID), Santa Ana, CA, USA
Publication Date: 1999 Country of Publication: USA CD-ROM pp.
Material Identity Number: XX-1999-01213
Conference Title: Proceedings of the 1999 SID International Symposium, Seminar & Exhibition
Conference Date: 18-20 May 1999 Conference Location: San Jose, CA, USA
Language: English
Abstract: The fixed charges in the **SiO** /sub 2/ underlying the poly-Si active layer was shown to have a significant effect on V/sub th/ of low temperature poly-Si TFT with **SiN**/sub x//**SiO**/sub 2/ dual under layer deposited by plasma enhanced chemical vapor deposition (PECVD). This effect is comparable to that of the charges in the gate

dielectric layer. Impurities of nitrogen in the **SiO**/sub 2/ cause the charges. The reduction of the nitrogen can stabilize V/sub th/ affected by fluctuations of deposition conditions.
Subfile: B

32/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6812211 INSPEC Abstract Number: B2001-02-2560R-110
Title: Thin film transistors of microcrystalline silicon deposited by plasma enhanced-CVD
Author(s): Chen, Y.; Wagner, S.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Conference Title: Amorphous and Heterogeneous Silicon Thin Films: Fundamentals to Devices - 1999. Symposium. (Materials Research Society Symposium Proceedings Vol.557) p.665-70
Editor(s): Branz, H.M.; Collins, R.W.; Okamoto, H.; Guha, S.; Schropp, R.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1999 Country of Publication: USA xviii+888 pp.
ISBN: 1 55899 464 5 Material Identity Number: XX-2000-00545
Conference Title: Amorphous and Heterogeneous Silicon Thin Films: Fundamentals to Devices - 1999. Symposium
Conference Date: 5-9 April 1999 Conference Location: San Francisco, CA, USA
Language: English
Abstract: We fabricated top gate TFTs of microcrystalline silicon (mu c-Si) deposited at 360 degrees C. The TFTs have field-effect electron mobilities of up to 7.9 cm/sup 2//Vs in the saturation regime and 5.8 cm/sup 2//Vs in the linear regime. The highest I/sub ON//I/sub OFF/ ratio is 10/sup 5/. Typical values for V/sub th/ is 6.5 V and for the subthreshold slope is 1.7 V/decade. The mu c-Si is grown by PE-CVD from a source gas mixture of SiH/sub 4/, SiF/sub 4/ and H/sub 2/, with a typical flow ratio of 1:20:200, at a pressure of 120 Pa and a power density of 160 mW/cm/sup 2/. The TFT structure is built on un-passivated Corning 7059 glass, with 300 nm mu c-Si, 60 nm n/sup +/ mu c-Si source and drain contact layers, 200 nm **SiO**/sub 2/ or 300 nm **SiN**/sub x/ gate **insulator**, and 100 nm Al gate, **source** and **drain electrodes**.
Subfile: B

32/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6812210 INSPEC Abstract Number: B2001-02-2560R-109
Title: Thin-film transistors based on hot-wire amorphous silicon on **silicon nitride**
Author(s): Stannowski, B.; Meiling, H.; Brockhoff, A.M.; Schropp, R.E.I.
Author Affiliation: Debye Res. Inst., Utrecht Univ., Netherlands
Conference Title: Amorphous and Heterogeneous Silicon Thin Films: Fundamentals to Devices - 1999. Symposium. (Materials Research Society Symposium Proceedings Vol.557) p.659-64
Editor(s): Branz, H.M.; Collins, R.W.; Okamoto, H.; Guha, S.; Schropp, R.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1999 Country of Publication: USA xviii+888 pp.
ISBN: 1 55899 464 5 Material Identity Number: XX-2000-00545

Conference Title: Amorphous and Heterogeneous Silicon Thin Films: Fundamentals to Devices - 1999. Symposium
Conference Date: 5-9 April 1999 Conference Location: San Francisco, CA, USA
Language: English
Abstract: We present state-of-the-art thin-film transistors (TFTs) incorporating amorphous silicon i-layers deposited by hot-wire chemical vapor deposition. The TFTs are deposited on glow-discharge **silicon nitride** as well as on thermally-grown **silicon dioxide**. The devices on **silicon nitride** have a field-effect mobility above 0.7 cm/sup 2//Vs, a threshold voltage around 2 V and a sub-threshold slope as low as 0.5 V/dec. As commonly observed, the TFTs on **silicon-dioxide** have higher values for the threshold voltage and the sub-threshold slope. In the annealed state the hot-wire TFTs show almost the same properties as TFTs deposited by conventional plasma-enhanced chemical vapor deposition. Nevertheless, the stress-time dependent behavior under prolonged gate-voltage stress at elevated temperature is different from that of the glow-discharge devices. The hot-wire TFTs are clearly more stable than their glow-discharge counterparts. Furthermore, we found differences in the stress behavior of the hot-wire TFTs deposited on **silicon nitride** and **silicon dioxide**.
Subfile: B

32/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6619254 INSPEC Abstract Number: B2000-07-2560R-100
Title: Amorphous silicon thin-film transistor with fluorinated **silicon oxide** ion stopper
Author(s): Kyung Wook Kim; Kyu Sik Cho; Jai Il Ryu; Keon Ho Yoo; Jin Jang
Author Affiliation: Dept. of Phys., Kyung Hee Univ., Seoul, South Korea
Journal: IEEE Electron Device Letters vol.21, no.6 p.301-3
Publisher: IEEE,
Publication Date: June 2000 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200006)21:6L.301:ASTF;1-#
Material Identity Number: I338-2000-006
U.S. Copyright Clearance Center Code: 0741-3106/2000/$10.00
Language: English
Abstract: We propose fluorinated **silicon oxide** (SiOF) as the ion-stopper of bottom-gate amorphous silicon thin film transistors (a-Si:H TFTs). The low **dielectric** constant SiOF on both the back-channel of the TFT and the crossover regions of gate/data lines can contribute to reducing the RC delay of the gate pulse signal in active-**matrix liquid-crystal** displays. Besides, the a-Si:H TFT with a SiOF stopper shows an improved performance compared to the widely-employed **silicon nitride** (**SiN** /sub x/) stopper TFT, because the fluorine incorporation reduces the interface state density between a-Si:H and SiOF.
Subfile: B

32/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5690433 INSPEC Abstract Number: B9710-2560R-050

Title: Investigation of the off-current in amorphous silicon thin film transistors for **SiO**/sub 2/ and **SiN**/sub x/ gate **insulators**
Author(s): Jeong Hyun Kim; Woong Sik Choi; Chan Hee Hong; Hoe Sup Soh
Author Affiliation: LG Electron. Inc., Kyungkido, South Korea
Conference Title: Flat Panel Display Materials II. Symposium p.85-90
Editor(s): Hatalis, M.K.; Kanicki, J.; Summers, C.J.; Funada, F.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1997 Country of Publication: USA xiii+513 pp.
Material Identity Number: XX97-00780
Conference Title: Flat Panel Display Materials II. Symposium
Conference Date: 8-12 April 1996 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The off current behavior of hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) with an atmospheric pressure chemical vapor deposition (APCVD) **silicon dioxide** (**SiO**/sub 2/) gate **insulator** were investigated at negative gate voltages. The a-Si:H TFT with **SiO**/sub 2/ gate **insulator** has small off currents and large activation energy (E/sub a/) of the off current compared to the a-Si:H TFT with **SiN**/sub x/ gate **insulator**. The holes induced in the channel by negative gate voltage seem to be trapped in the defect states near the a-Si:H/**SiO**/sub 2/ interface. The interface state density in the lower half of the band gap of a-Si:H/**SiO**/sub 2/ appears to be much higher than that for a-Si:H/**SiN**/sub x/.
Subfile: B

32/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5100689 INSPEC Abstract Number: A9523-8115H-028, B9512-0520F-086
Title: High deposition rate PECVD processes for next generation TFT-LCDs
Author(s): Westendorp, J.F.M.; Meiling, P.; Pollock, J.D.; Berrian, D.W.; Laflamme, A.H., Jr.; Hautala, J.; Vanderpot, J.
Author Affiliation: TEL America Inc., Beverly, MA, USA
Conference Title: Flat Panel Display Materials. Symposium p.175-83
Editor(s): Batey, J.; Chiang, A.; Holloway, P.H.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA ix+339 pp.
Conference Title: Flat Panel Display Materials. Symposium
Conference Date: 5-6 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The demand for lower cost per panel in TFT-**LCD** production is driving demand for PECVD systems that combine high throughput and uptime with high yield. It is generally believed that a multichamber system combining a number of single-panel deposition chambers is the best way to achieve these goals. For these systems to be economical, the deposition rate of a-Si:H, **SiN**/sub x/ and **SiO** /sub 2/ must be in the 1200-1500 AA/min range. In 13.56 MHz parallel-plate glow discharge systems, **SiN**/sub x/ and **SiO** /sub 2/ deposition rates exceeding 1500 AA/min are commonly achieved, whereas the deposition rate of a-Si:H is limited to 100-200 AA/min due to powder formation. Over the last 5 years, significant progress has been made in increasing the a-Si:H deposition rate. Methods include VHF glow discharge (VHF-GD) and RF discharge pulsing, but substrate sizes never exceeded 100 mm*100 mm. We have developed a multichamber PECVD system for TFT-**LCD** production where VHF-GD is used to obtain uniform high deposition rates for (doped) semiconductors and **insulators**, such as a-Si:H, n/sup +/-a-Si:H, **SiN**/sub x/ and

SiO /sub 2/ over areas as large as 470 mm*370 mm. Even at deposition rates well above 1200 AA/min, hydrogen in a-Si:H is exclusively bound as monohydride. The optoelectronic properties of the films are at least as good as those of their 13.56 MHz counterparts and thus good-quality TFTs can be obtained. At the same time the number of added particles is low, allowing for high production yield.
Subfile: A B

32/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5058456 INSPEC Abstract Number: B9511-2570H-002
Title: Considerations for large area fabrication of integrated a-Si and poly-Si TFTs
Author(s): Mei, P.; Anderson, G.B.; Boyce, J.B.; Fork, D.K.; Hack, M.; Johnson, R.I.; Lujan, R.A.; Ready, S.E.
Author Affiliation: Xerox Palo Alto Res. Center, CA, USA
Conference Title: Amorphous Silicon Technology - 1994. Symposium p. 781-6
Editor(s): Schiff, E.A.; Hack, M.; Madam, A.; Powell, M.; Matsuda, A.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA xix+903 pp.
Conference Title: Amorphous Silicon Technology - 1994. Symposium
Conference Date: 4-8 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The combination of a-Si low leakage pixel TFTs with poly-Si TFTs in peripheral circuits provides an excellent method for reducing the number of external connections to large-area imaging arrays and displays. To integrate the fabrication of the peripheral poly-Si TFTs with the a-Si pixel TFTs, we have developed a three-step laser process which enables selective crystallization of PECVD a-Si:H. X-ray diffraction and transmission electron microscopy show that the polycrystalline grains formed with this three-step process are similar to those crystallized by a conventional one step laser crystallization of unhydrogenated amorphous silicon. The grain size increases with increasing laser energy density up to a peak value of a few microns. The grain size decreases with further increases in laser energy density. The transistor field effect mobility is correlated with the grain size, increasing gradually with laser energy density until reaching its maximum value. Thereafter, the transistors suffer from leakage through the gate **insulators**. A dual **dielectric** gate **insulator** has been developed for these bottom-gate thin film transistors to provide the correct threshold voltages for both a-Si and poly-Si TFTs.
Subfile: B

32/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

4775686 INSPEC Abstract Number: B9411-2560R-040
Title: a-Si TFTs with stacked gate **insulator** of CVD-**SiO**/sub 2//PECVD-**SiN**/sub x/
Author(s): Fukuda, K.; Ibaraki, N.
Author Affiliation: Electron Device Eng. Lab., Toshiba Corp., Yokohama, Japan

Journal: Electronics and Communications in Japan, Part 2 (Electronics) vol.76, no.12 p.11-19
Publication Date: Dec. 1993 Country of Publication: USA
CODEN: ECJEEJ ISSN: 8756-663X
U.S. Copyright Clearance Center Code: 8756-663X/93/0012-0011
Language: English
Abstract: a-Si thin-film transistors (TFTs) with a stacked gate **insulator** of thermal CVD-**SiO**/sub 2//PECVD-**SiN**/sub x/ were developed. In an a-Si TFT, the threshold voltage (V/sub th/) shifts when the gate is biased for a long time. The stability of V/sub th/, is influenced strongly by the characteristic of the gate **insulator**. Therefore, the high quality of the gate **insulator** is essential to achieve high performance in a TFT. When an **SiO**/sub 2/ film is formed by thermal CVD, the invasion of nitrogen to the **SiO**/sub 2/ film is minimized and the defect density is lower than in plasma-enhanced chemical vapor deposition (PECVD)-**SiO** /sub 2/. The properties of a TFT are strongly dependent on the **SiO**/sub 2/ deposition temperature and are improved by increasing the deposition temperature. When the gate **SiO** /sub 2/ was deposited at 430 degrees C, the field effect mobility mu was about 1 cm/sup 2//Vs and the V/sub th/ shift was greatly reduced. It is expected that the V/sub t/h shift in a TFT with a thermal **SiO**/sub 2/ gate for **LCD** driving is one-third that in a TFT with a PECVD-**SiO** /sub x/N/sub y/ gate used for the same purpose. Using the former TFTs, the time-dependent degradation of **LCD** due to the degradation of the subthreshold characteristic of TFTs was largely reduced.
Subfile: B

32/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

4598732 INSPEC Abstract Number: B9403-2560R-069
Title: a-Si thin film transistors using dilute-gas plasma-enhanced chemical vapor deposition
Author(s): Wright, S.L.; Rothwell, M.B.; Souk, J.H.; Kuo, J.
Author Affiliation: IBM T. J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: IEEE Transactions on Electron Devices vol.40, no.11 p. 2128-9
Publication Date: Nov. 1993 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/93/$03.00
Conference Title: IEEE 51st Annual Device Research Conference
Conference Sponsor: IEEE
Conference Date: 21-23 June 1993 Conference Location: Santa Barbara, CA, USA
Language: English
Abstract: Summary form only given. Dilute-gas plasma-enhanced chemical vapor deposition (PECVD) has been used to fabricate high-quality amorphous silicon (a-Si) thin film transistors (TFTs) which are suitable for active-**matrix liquid-crystal** displays. All PECVD layers were deposited using silane diluted to 2% in He or H/sub 2/, which greatly reduces the explosion hazards associated with silane. The quality of a-Si produced by low-power, He-diluted silane at rates of approximately 1 AA/s is comparable to that made with pure silane. He dilution has also been utilized to control the properties of **SiO**/sub 2/ and **SiN**/sub x/ **insulators** deposited by PECVD. Using this approach, the effects of several material aspects on TFT characteristics were examined. The TFT structures were bottom-gate, inverted-staggered devices with deposited n/sup +/ microcrystalline silicon contacts.

03/25/2003

Subfile: B

32/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

04363946 INSPEC Abstract Number: B9304-7260-025
Title: Process techniques of 15-inch full-color high-resolution **liquid crystal** displays addressed by a-Si thin film transistors
Author(s): Fujii, K.; Tanaka, Y.; Honda, K.; Tsutsu, H.; Koseki, H.; Hotta, S.
Author Affiliation: Matsushita Electric Ind. Co. Ltd., Ishikawa, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.31, no.12B p.4574-8
Publication Date: Dec. 1992 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
Language: English
Abstract: A 15 inch-diagonal-size full-color **liquid crystal** display (**LCD**) with 1152(*3)*900 pixels has been fabricated which enables a portable workstation with improved display performances. The process techniques used for this development are described, with special reference to metallization and dry etching. In **multilevel** metallization, Cr/Al interconnection is metallurgically undesirable. In contrast, the Cr/Ti/Al metal system provides excellent properties of contact resistivity and thermodynamical stability. Dry etching processes are developed for **multilayered insulating** films and metallization-related bilayers, namely **SiO**/sub 2//TaO/sub x// **SiN** /sub x//(i/n/sup +/)a-Si and a-Si/Ti, respectively. Fine patterning and easier stepcoverage of subsequently deposited layers are achieved.
Subfile: B

32/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

04336522 INSPEC Abstract Number: B9303-4250-016
Title: Ferroelectric **liquid crystal** light valve using **SiO**/sub 2//A-Si:H photodiode
Author(s): Horikawa, T.; Tahata, S.; Kaho, S.; Masumi, T.; Mikami, N.; Takahashi, K.; Nunoshita, M.; Nakajima, H.; Nishi, K.
Author Affiliation: Mitsubishi Electric Corp., Hyogo, Japan
Conference Title: Amorphous Silicon Technology - 1991 Symposium p. 203-8
Editor(s): Madan, A.; Hamakawa, Y.; Thompson, M.J.; Taylor, P.C.; LeComber, P.G.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1991 Country of Publication: USA xx+884 pp.
Conference Date: 30 April-3 May 1991 Conference Location: Anaheim, CA, USA
Language: English
Abstract: A new type of ferroelectric **liquid crystal** light valve (FLCLV) is presented. The design of the FLCLV is based upon the linear equivalent circuit analyses. A photosensor in the FLCLV consists of a metal-**insulator** -semiconductor (MIS) photodiode. A-Si:H doped with boron and nitrogen (a-**Si**:(:**N**:B)) is used in the MIS diode. The a-Si:H(:B:N) film has a dark-conductivity of less than 1*10/sup -12/ S/cm and a high photosensitivity. Consequently, the writing characteristics of the FLCLV for a two dimensional (2D) image are evaluated. Using writing

light of 630 nm and 1 mW/cm/sup 2/, a high resolution capability of 120 approximately 140 lp/mm is obtained.
Subfile: B

32/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

04332146 INSPEC Abstract Number: B9303-2560R-036
Title: Polycrystalline-silicon thin-film transistors with low-temperature gate dielectrics
Author(s): Huang-Chung Cheng; Jau-Jey Wang; Ya-Hsiang Tai; Ming-Shiang Feng
Author Affiliation: National Chiao Tung Univ., Hsinchu, Taiwan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1815 p.146-50
Publication Date: 1992 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
U.S. Copyright Clearance Center Code: 0 8194 1015 2/92/$4.00
Conference Title: Display Technologies
Conference Sponsor: Nat. Chiao Tung Univ.; SPIE
Conference Date: 17-18 Dec. 1992 Conference Location: Hsinchu, Taiwan
Language: English
Abstract: Thin-film transistors (TFTs) have been fabricated by using low-pressure chemical vapor deposition (LPCVD) polycrystalline-silicon (poly-Si) film as the active layer. Various gate dielectrics, i.e. high-temperature gate oxides with different thicknesses, low-temperature thin gate oxides, different combinations of oxide/nitride (O/N) structures with various thicknesses, as well as low-temperature oxide/nitride gate dielectrics have been performed. Their effect on the poly-Si TFTs were investigated. The effective carrier mobility of the devices with thin gate oxides are several times larger than those with thick gate oxides. However, the breakdown voltages of thin gate oxides are too low to satisfy the requirements of TFTs. **Silicon nitride** deposited by LPCVD can be a substitution due to low fabrication temperatures (700 degrees C to 900 degrees C), high breakdown field, and smooth **dielectric**/poly-Si interfaces, but the problem of adopting **silicon nitride** is the large stress between **silicon nitride** and silicon substrate. A thin thermal pad oxide beneath the **silicon nitride** was therefore grown in order to reduce the high stress at the interface between **silicon nitride** and poly-Si layer of TFTs. The optimum thickness of pad oxide is found to be 100 AA. Hence, high-performance TFTs with O/N gates can be fabricated at the processing temperatures below 800 degrees C to satisfy the requirements of TFTs in the **liquid crystal** displays (LCDs).
Subfile: B

32/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

04236268 INSPEC Abstract Number: B9210-2560R-060
Title: Study of the V/sub th/ shift of the thin-film transistor by the bias temperature stress test
Author(s): Fujimoto, Y.
Author Affiliation: IBM Japan, Display Technol., Kanagawa, Japan
Journal: IBM Journal of Research and Development vol.36, no.1 p. 76-82
Publication Date: Jan. 1992 Country of Publication: USA

CODEN: IBMJAE ISSN: 0018-8646
Language: English
Abstract: Amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as the switching device in the active-**matrix** addressing of **liquid crystal** displays. One concern is the potential instability problems associated with the threshold voltage (V/sub th/) shifts to higher values after prolonged operating times. The reason for this V/sub th/ shift has been widely discussed, and two models accounting for it have been suggested. One model explains the shifts by the trapping of electrons in the **insulator**, the other model by the creation of the metastable states at the a-Si:H/**SiN**/sub x/ interface. The author's TFT **insulator** has the rather complicated structure of an anodic oxide film, **SiO**/sub x/, **SiN**/sub x/ sequentially stacked over the **gate electrode** , which makes it difficult to separate the contribution of each layer. To confirm the V/sub th/ shift mechanism and the contribution of each layer of **insulator** to the V/sub th/ shift, he prepared samples with a series of different **insulators** and measured the bias dependence of their V/sub th/ shifts. His results show that the anodic oxide film makes no contribution to the V/sub th/ shift, and it makes little difference to the V/sub th/ shift whether the next **insulator** is **SiN**/sub x/ or **SiO**/sub x/.
Subfile: B

32/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

04234144 INSPEC Abstract Number: B9210-2560R-054
Title: A new a-Si TFT with **SiO**/sub 2//**SiN**/sub x/ gate **insulator** for 10.4-inch LCDs
Author(s): Ibaraki, N.; Shimano, T.; Fukuda, K.; Matsumura, K.; Suzuki, K.; Toeda, H.; Takikawa, O.
Author Affiliation: Toshiba Corp., Yokohama, Japan
Conference Title: Conference Record of the 1991 International Display Research Conference (Cat. No.91CH3071-8) p.97-100
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA vii+257 pp.
ISBN: 0 7803 0213 3
U.S. Copyright Clearance Center Code: CH3071-8/91/0000-0097$01.00
Conference Sponsor: IEEE; SID; Advisory Group Electron Devices
Conference Date: 15-17 Oct. 1991 Conference Location: San Diego, CA, USA
Language: English
Abstract: A novel a-Si TFT (thin-film transistor) with a composite gate **insulator** of CVD (chemical-vapor-deposited) **SiO**/sub 2//PE-CVD (plasma-enhanced CVD) **SiN** /sub x/ has been developed. This TFT has been applied to 10.4-in-diagonal LCDs (**liquid crystal** displays). Because of the high quality of CVD **SiO**/sub 2/, Vth drift, which was often observed after prolonged application of gate bias, was remarkably reduced compared to PE-CVD **SiO**/sub x/N/sub y/. Also, the degradation of subthreshold characteristics on a-Si TFT (often observed after long-term operation of LCDs at high temperature) was improved. Selective etching technologies of **SiN**/sub x/ against **SiO**/sub 2/, which is one of key issues in connection with obtaining high production yield, have been developed.
Subfile: B

32/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

04126657 INSPEC Abstract Number: B9205-0520F-025
Title: Plasma enhanced CVD for flat panel displays
Author(s): Corwley, J.L.
Author Affiliation: O'Mara & Associates, Palo Alto, CA, USA
Journal: Solid State Technology vol.35, no.2 p.94-7
Publication Date: Feb. 1992 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
Language: English
Abstract: Plasma enhanced chemical vapor deposition (PECVD) is the preferred deposition method for many thin films used in active **matrix liquid crystal** flat panel displays (AMLCD). It is especially suited for depositing the hydrogenated amorphous silicon (alpha -Si:H) active semiconductor layer and is also used to deposit gate and field **dielectric** thin films such as **SiN**/sub x/ and **SiO**/sub 2/. This article reviews PECVD with respect to film properties, processes, and equipment for flat panel displays.
Subfile: B

32/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

03564114 INSPEC Abstract Number: B90018634
Title: Flat LC direct panel- and projection-displays with CdSe- and with a-Si thin film transistors
Author(s): Luder, E.; Schwarz, F.; Kallfass, T.; Spachmann, J.; Otterbach, W.
Author Affiliation: Stuttgart Univ., West Germany
Journal: ITG-Fachberichte vol.108 p.11-15
Publication Date: 1989 Country of Publication: West Germany
CODEN: ITGFEY ISSN: 0341-0196
Language: German
Abstract: In thin film transistors based on CdSe or a-Si as semiconductor, the stability and current delivery are enhanced by including in the structure a double layer gate **dielectric** of Ta/sub 2/O/sub 5/ and **SiO**/sub 2/, or **SiN** . The manufacturing of both types is compared step-by-step. TFT controlled TN-LC direct view displays with 12880 Pel have a 1:48 contrast. Projection displays shown no grey mist even with 80 pictures/sec., because the TFT addressed TN cell switches rapidly: in-10 ms, out-25 ms. An optical low pass greatly reduces the visibility of driving lines.
Subfile: B

32/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

03319409 INSPEC Abstract Number: A89026752, B89013698
Title: Extended Abstracts of the Fall Meeting of the Electrochemical Society
Publisher: Electrochem. Soc, Manchester, NH, USA
Publication Date: 1988 Country of Publication: USA xli+1081 pp.
Conference Date: 9-14 Oct. 1988 Conference Location: Chicago, IL, USA
Language: English
Abstract: The following topics were dealt with: mathematical models applied to batteries; lithium batteries; fuel cell technology; corrosion; nuclear waste container corrosion; metallized plastics; isolation and

trench technology; **multilevel** metallization, interconnection and contact technologies; **silicon nitride** and **silicon dioxide** thin **insulating** films; semiconductor device and interconnection reliability; electroplating process modelling; electrodeposits; semiconductor electrodeposition; beam testing of circuits and devices; automated IC manufacturing; diagnostic techniques for semiconductor materials and devices; focused ion beam technology; heteroepitaxy in semiconductors; environmental effects of energy systems; high temperature corrosion; chemical interactions in high temperature composites; luminescence science and technology; optical imaging; photonics; X-ray imaging; optical sensors; magnetic field effects in electrochemistry; tunnelling microscopy and related techniques; electrochemistry in semiconductor technology; ionic motion in solid state materials; sensors.
Subfile: A B

32/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

01611891 INSPEC Abstract Number: B81003518
Title: Light barrier for integrated projection display
Author(s): Huntley, F.A.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.23, no.1 p.347-8
Publication Date: June 1980 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: In an electrochromic or **liquid crystal** projection display in which an array of reflective display electrodes is formed on a silicon substrate, the gaps between the electrodes may permit light to penetrate towards the substrate. If such light were to reach the silicon, the resulting photoconduction could produce undesirable electrical leakage paths within the integrated display. It is shown that a light barrier can be formed conveniently as a **multilayer dielectric** mirror during fabrication of the integrated display device. This **dielectric** mirror is formed by reactive plasma deposition of alternate thin layers of **silicon oxide** and **silicon nitride**.
Subfile: B

32/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

00670820 INSPEC Abstract Number: B74030014
Title: Characterization of localized defects in **dielectric** films for electron devices. II
Author(s): Kern, W.
Author Affiliation: RCA Corp., Princeton, NJ, USA
Journal: Solid State Technology vol.17, no.4 p.78-84
Publication Date: April 1974 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
Language: English
Abstract: For pt. I see ibid., vol.17, 35-42 (1974). Capabilities and limitations of various types of analytical methods for detecting and characterizing localized imperfections in typical **dielectric** films used in present-day silicon semiconductor device technology are surveyed and compared. Dielectrics and **insulators** of particular interest include thermally grown **silicon dioxide** and layers of vapor

deposited **silicon dioxide**, silicate glasses, **silicon nitride**, aluminum oxide, and complex silicates in thicknesses ranging from several hundred angstroms to several micrometers. The analytical methods discussed in some detail include optical contrast microscopy, scanning electron microscopy, self-healing **dielectric** breakdown, selective chemical etching, electrolytic decoration, **liquid crystal** techniques, electron-probe microanalysis, and ion microprobe mass analysis. Several additional methods are briefly noted. Particular emphasis is placed on recent improvements achieved in these analytical methods. Applications are discussed and illustrated with typical examples, and trends in future developments are indicated.
Subfile: A B

32/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

00660009 INSPEC Abstract Number: A74049621, B74026377
Title: Characterization of localized defects in **dielectric** films for electron devices. I
Author(s): Kern, W.
Author Affiliation: RCA Corp., Princeton, NJ, USA
Journal: Solid State Technology vol.17, no.3 p.35-42
Publication Date: March 1974 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
Language: English
Abstract: Capabilities and limitations of various types of analytical methods for detecting and characterizing localized imperfections in typical **dielectric** films used in present-day silicon semiconductor device technology are surveyed and compared. Dielectrics and **insulators** of particular interest include thermally grown **silicon dioxide** and layers of vapor deposited **silicon dioxide**, silicate glasses, **silicon nitride** , aluminum oxide, and complex silicates in thicknesses ranging from several hundred angstroms to several micrometers. The analytical methods discussed in some detail include optical contrast microscopy, scanning electron microscopy, self-healing **dielectric** breakdown, selective chemical etching, electrolytic decoration, **liquid crystal** techniques, electron-probe microanalysis, and ion microprobe mass analysis. Several additional methods are briefly noted. Particular emphasis is placed on recent improvements achieved in these analytical methods. Applications are discussed and illustrated with typical examples, and trends in future developments are indicated.
Subfile: A B

32/3,AB/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

00637832 INSPEC Abstract Number: A74037132, B74018718
Title: Detection and characterization of localized defects in **dielectric** films
Author(s): Kern, W.
Author Affiliation: RCA Labs., Princeton, NJ, USA
Journal: RCA Review vol.34, no.4 p.655-90
Publication Date: Dec. 1973 Country of Publication: USA
CODEN: RCARCI ISSN: 0033-6831
Language: English
Abstract: Capabilities and limitations of various types of analytical methods for detecting and characterizing localized imperfections in typical

dielectric films used in present-day silicon semiconductor device technology are surveyed and compared. Dielectrics and **insulators** of particular interest include thermally grown **silicon dioxide** and layers of vapor-deposited **silicon dioxide**, silicate glasses, **silicon nitride** , aluminum oxide, and complex silicates. The preparation and application of these materials are briefly surveyed, and frequently encountered defects and some of their causes are reviewed. The analytical methods discussed in some detail include optical contrast microscopy, scanning electron microscopy, self-healing **dielectric** breakdown, selective chemical etching, electrolytic decoration, **liquid-crystal** techniques, electron-probe microanalysis, and ion microprobe mass analysis. Applications are discussed and illustrated with typical examples, and trends in future developments are indicated.
Subfile: A B

32/3,AB/23 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1040718 NTIS Accession Number: PB83-209965
Reports of the Research Laboratory, Asahi Glass Co., Ltd. Volume 32, Number 1, 1982
Asahi Glass Co. Ltd., Yokohama (Japan). Research Lab.
Corp. Source Codes: 076427001
1982 73p
Languages: English
Journal Announcement: GRAI8318
See also Volume 31, Number 2, PB83-101865. Color illustrations reproduced in black and white.
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NTIS Prices: PC A04/MF A01
This issue contains six reports from the Research Laboratory. All reports have an English Abstract with English text as noted. The contents are: Mechanical properties of **silica** films evaporated on Columbia Resin CR-39 (Japanese); Improvement of **LCD** legibility for automobiles (English); Strength distribution of sintered **silicon nitride** (English); Zirconia fusion cast refractory (Japanese); The determination of very small amount of tin in lead glass by atomic absorption spectrometry (Japanese); Polyphenylene sulfide for electrical **insulation** use (Japanese).

32/3,AB/24 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05589829
E.I. No: EIP00065218738
Title: Amorphous silicon thin-film transistor with fluorinated **silicon oxide** ion stopper
Author: Kim, Kyung Wook; Cho, Kyu Sik; Ryu, Jai Il; Yoo, Keon Ho; Jang, Jin
Corporate Source: Kyung Hee Univ, Seoul, South Korea
Source: IEEE Electron Device Letters v 21 n 6 2000. p 301-303
Publication Year: 2000
CODEN: EDLEDZ ISSN: 0741-3106
Language: English

Abstract: We propose fluorinated **silicon oxide** (SiOF) as the ion-stopper of bottom-gate amorphous silicon thin film transistors (a-Si:H TFT's). The low **dielectric** constant SiOF on both back-channel of the TFT and the crossover regions of gate/data lines can contribute to reducing the RC delay of the gate pulse signal in active-**matrix liquid-crystal** displays. Besides, an a-Si:H TFT with a SiOF stopper had an improved performance compared to a widely-employed **silicon nitride** (**SIN**//x) stopper TFT because the fluorine incorporation reduces the interface state density between a-Si:H and SiOF. (Author abstract) 10 Refs.

32/3,AB/25 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04049933
E.I. No: EIP95012529895
Title: Effects of N//2 plasma treatment on **SiO**//2 gate **insulator** in a-Si:H thin film transistor
Author: Kim, Sung Chul; Bai, Sung Sig; Oh, Eui Yeol; Kim, Jeong Hyun; Lee, Jong Wan; Kim, Cha Yeon; Kim, Donggil
Corporate Source: GoldStar Co, Ltd, Kyongki-do, South Korea
Conference Title: Proceedings of the 1994 MRS Spring Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19940405-19940406
E.I. Conference No.: 42268
Source: Materials Research Society Symposium Proceedings 345 1994. p 29-34
Publication Year: 1994
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Abstract: We fabricated the high performance a-Si:H TFT using the N//2 plasma treated APCVD **SiO**//2 as a gate **insulator**. The effects of N//2 plasma treatment on the APCVD **SiO**//2 were investigated by XPS and SIMS measurements. And the formation of the oxynitride interface layer between a-Si:H and APCVD **SiO**//2 was found in the a-Si:H TFT. From our experimental results, It may be concluded that most nitrogen atoms, which were incorporated by the exposure of **SiO**//2 layer to N//2 plasma, exist, not bonded to other atoms, near the surface of the **SiO**//2 layer and during the sequential deposition of a-Si:H on the N//2 plasma treated APCVD **SiO**//2 layer **Si-N** bonds are formed, resulting in the oxynitride layer in the interface region. This explains the high performance a-Si:H TFT with the N//2 plasma treated APCVD **SiO**//2 gate **insulator**. (Author abstract) 8 Refs.

32/3,AB/26 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03523256
E.I. Monthly No: EI9212161966
Title: Study of the V//t//h shift of the thin-film transistor by the bias temperature stress test.
Author: Fujimoto, Y.
Corporate Source: IBM Japan, Yamato, Jpn
Source: IBM Journal of Research and Development v 36 n 1 Jan 1992 p 76-82
Publication Year: 1992
CODEN: IBMJAE ISSN: 0018-8646
Language: English

Abstract: Amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as the switching device in the active-**matrix** addressing of **liquid crystal** displays. One concern is the potential instability problems associated with the threshold voltage (V//t//h) shifts to higher values after prolonged operating times. The reason for this V//t//h shift has been widely discussed, and two models accounting for it have been suggested. One model explains the shifts by the trapping of electrons in the **insulator**, the other model by the creation of the metastable states at the a-Si:H/**SiN**//x interface. Our TFT **insulator** has the rather complicated structure of an anodic oxide film **SiO**//x, **SiN**//x sequentially stacked over the **gate electrode**, which makes it difficult to separate the contribution of each layer. To confirm the V//t//h shift mechanism and the contribution of each layer of **insulator** to the V//t//h shift, we have prepared samples with a series of different **insulators** and have measured the bias dependence of their V//t//h shifts. Our results show that the anodic oxide film makes no contribution to the V//t//h shift, and it makes little difference to the V//t//h shift whether the next **insulator** is **SiN**//x or **SiO**//x. The latter fact may be explained in two ways. One is that both **SiN**//x and **SiO**//x make the same contribution to the V//t//h shift. Alternatively, neither **SiN**//x nor **SiO**//x makes any contribution to the V//t//h shift, but the a-Si:H/gate **insulator** interface has some contribution. From these experiments, it cannot be determined which of the proposed mechanisms is consistent with the behavior of the V//t//h shift of our a-Si:H TFT. (Author abstract) 7 Refs.

32/3,AB/27 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02941811
E.I. Monthly No: EI9008098570
Title: Amorphous silicon thin-film transistors with **SiO**//xN//y/**SiN**//x gate **insulators**.
Author: Hiranaka, Kouichi; Yamaguchi, Tadahisa
Corporate Source: Fujitsu Lab Ltd, Atsugi, Jpn
Source: Japanese Journal of Applied Physics, Part 1: Regular Papers & Short Notes v 29 n 2 Feb 1990 p 229-235
Publication Year: 1990
CODEN: JAPNDE ISSN: 0021-4922
Language: English
Abstract: A double layer of plasma chemical vapor deposition **SiO**//xN//y and **SiN**//x was applied to the gate **insulator** of an amorphous silicon (a-Si) thin-film transistor (TFT). When a thin **SiN**//x layer is inserted between the a-Si of an a-Si TFT and the **SiO**//xN//y gate **insulator**, the density of trapped charges is found to decrease less than for a gate **insulator** with only **SiN**//x, when the thickness of **SiN**//x is decreased. No deterioration was observed in the switching characteristics of an a-Si TFT with a **SiO**//xN//y/**SiN**//x gate **insulator**, compared with a-Si TFTs with **SiN**//x gate **insulators** commonly used in **liquid crystal** displays. The density of trapped charges is related to the threshold voltage shift. (Author abstract) 17 Refs.

32/3,AB/28 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

03/25/2003

01843128 AADAAI3021358
A study of low-temperature, diethysilane-based, chemical vapor deposited **silicon oxide** as a bulk and thin film metal-oxide-semiconductor gate **dielectric**
Author: Chen, Danny Li-Ping
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: Cornell University (0058)
Source: VOLUME 62/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3340. 187 PAGES
ISBN: 0-493-32036-9

Low-temperature silicon oxides (LTO) are required for gate and interlevel **dielectric** applications when thermal budget constraints rule out the use of high-temperature processes such as thermal oxidation. The increase in the number of metallization layers in integrated circuits, and the application of thin film transistor (TFT) in **liquid crystal** flat panel display drivers, SOI-DRAM, and 3-D repeater circuit technologies all have spurred increasing research into the optimal processing of LTO.

To investigate the properties of LTO deposited from diethylsilane at 450°C, MOS capacitors were fabricated to measure the interface charge states at the LTO/silicon interface that may lead to device instabilities. Densification of LTO up to 600°C in various ambient reduced the oxide charges and resulted in C-V behavior approaching ideal conditions as seen in thermal oxides. LTO breakdown field and charge conduction were measured and shown to also improve with densification. Changes in the LTO etch rate, density, stress, ellipsometry, and composition accompanying densification were investigated to better understand how the densification process improves the electrical performance. The densification process was found to have a 2-Zone behavior showing that the densification process repairs defects rapidly and saturates at higher annealing temperatures.

Polycrystalline Si transistors on glass use deposited gate dielectrics, as glass cannot withstand the temperatures required to grow a thermal oxide. Fabrication of improved silicon as a channel material requires understanding and control of the trapping states present at grain boundaries, inside crystallites, or at the gate **dielectric**/poly-Si interface. To develop better understanding of these factors, the previous C-V analysis of LTO on single crystal silicon was extended to LTO deposited on LPCVD poly-Si thin films. This work presents a novel, systematic approach that employs the MOPS (metal-oxide-poly-Si-Si) structure to electrically evaluate the traps present at the interface and inside the poly-Si via a combination of high frequency and quasistatic frequency C-V. The poly-Si trap density can be quantified and the effectiveness of the hydrogenation process can be monitored.

Lastly, poly-Si TFTs using densified LTO were fabricated. These TFTs used a novel hydrogenation method to passivate poly-Si trap states that employs dual encapsulation of the active device area with PECVD **silicon nitride** that yields transistor characteristics comparable to a state of the art ECR process.

32/3,AB/29 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01712308 AADAAI9946434
Advanced gate dielectrics for thin film and CMOS transistors
Author: Klein, Tonya Micah
Degree: Ph.D.
Year: 1999

Corporate Source/Institution: North Carolina State University (0155)
Source: VOLUME 60/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4744. 134 PAGES

As semiconductor device technology evolves, the industry continues to place more stringent limits on the acceptable physical and electrical properties of materials used to make transistors. Of these materials, the gate **dielectric** is one of the most critical to thin film and CMOS transistor performance. We have investigated very low temperature (<150°C) plasma enhanced chemical vapor deposited hydrogenated **silicon nitride**, **SiN**_xH_y, as the gate **dielectric** in thin film transistors used in **liquid crystal** displays. Traditionally deposited at 300–400°C, the development of good quality <150°C **silicon nitride** thin films would allow the manufacture of these displays on rugged, flexible, transparent plastics. Silane and nitrogen are used as the reactants while helium is used as a diluent. The addition of helium enabled the control of the film stoichiometry so that similar films could be made at low temperatures as at higher temperatures. The affect of He on the plasma chemistry was monitored using optical emission spectroscopy and mass spectrometry and a plasma kinetic model was developed to predict film property trends. Complementary metal oxide semiconductor, CMOS, transistors, used in logic chips, are made with thermally grown **SiO**₂ as the gate **dielectric**. The dimensions of these devices are continuously scaled down to make chips faster and cheaper. Within 10 years the thickness of the **SiO**₂ (k = 4) gate **dielectric** is expected to decrease from 30 Å to less then 15 Å. At this thickness the tunneling of electrons will be too excessive for transistor operation. For continued transistor dimension scaling, an alternate high **dielectric** constant **insulator** is necessary. We have deposited Ta₂O₅ and Al₂O₃ (k = 25 and 12 respectively) thin films using metal organic chemical vapor deposition from various precursors and have characterized them using transmission infra-red spectroscopy and current vs. voltage/capacitance vs. voltage electrical measurements on metal/oxide/semiconductor (MOS) devices. The feasibility of the use of these materials in future technology will be discussed.

32/3,AB/30 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01462515 AADAAI9604565
PHYSICS, TECHNOLOGY AND CHARACTERIZATION OF POLYSILICON THIN FILM TRANSISTORS WITH LOW LEAKAGE CURRENT PERFORMANCE

Author: LIN, SU-HENG
Degree: PH.D.
Year: 1995
Corporate Source/Institution: LEHIGH UNIVERSITY (0105)
Source: VOLUME 56/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 5681. 223 PAGES

We investigate a new device structure without complicated processing steps in order to improve the leakage current while maintaining the high drive current of polysilicon thin film transistors (poly-Si TFTs). First of all, we establish a quantitative relationship between leakage current and applied biases, e.g. gate bias and drain bias. The effect of electric field on the emission of carriers from traps within the drain depletion region are considered in this new analytical model. A pseudo-two-dimensional analysis is adopted to simulate the electric field in poly-Si thin film

transistors. From simulation results of the analytical model we know how to play with those processing parameters in order to future improve the proposed device structure of poly-Si TFTs.

This proposed poly-Si TFT structure has an offset gate-to-drain region which is conductive due to the self-induced charges accumulated at the channel surface due to the incorporated charges inside the passivation layer above it. Two methods are used to introduce positive charges into the passivation layer of n-channel poly-Si TFTs: high frequency hydrogen plasma treatment and ion implantation. MOS capacitors were used to identify the introduced positive charge density, and its relationship to the processing parameters. It is proved that both methods can introduced positive charges into the passivation layer.

Four kinds of poly-Si TFT structures, including the proposed structure, were then fabricated and characterized in the Display Research Laboratory. Particular emphasis is given to the new offset gate TFT structure with self-induced drain and source regions. Hydrogen plasma treatment is applied to the self-induced conductive offset (SICO) poly-Si TFT at two different stages: during the fabrication of passivation layer and after post-metallization-annealing of the TFT. In the former processing we examine the effect of **dielectric** structures, e.g. single layer (**SiO**$\sb2)$ and double layer (**SiO**$\sb2$ + **SiN**$\sb{x}),$ on the electrical performance of poly-Si TFTs. In the latter processing we optimize the plasma parameters, e.g. power, pressure and temperature, used in hydrogen plasma treatment. Electrical properties, e.g. carrier mobility, threshold voltage, subthreshold swing, drive current and leakage current characteristics are mainly characterized. Furthermore, the uniformity of device characteristics is investigated as a function of device geometry and processing parameters. The result shows that the double-layer SICO poly-Si TFT exhibits the best ON/OFF current performance, i.e. an ON/OFF current ratio more than 10$\sp7,$ after the post-metallization hydrogen plasma treatment.

Activation energy of drain current is examined in the four kinds of TFT structures in order to verify the leakage current mechanism and the drive current improvement. The stability of poly-Si TFTs, particularly of the device leakage current, is also investigated under a steady state bias stress. As we expected, the DL-SICO structure has the best immunity to the bias stress as well as the thermal stress among the four kinds of poly-Si TFTs.

The successful development of SICO poly-Si TFTs encourage us to apply poly-Si TFTs in active **matrix liquid crystal** displays. A further research can emphasize the ion implantation technique which can provide positive charges for the n-channel devices and negative charges for the p-channel devices. (Abstract shortened by UMI.)

32/3,AB/31 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03471566 JICST ACCESSION NUMBER: 98A0016683 FILE SEGMENT: JICST-E
Charging of glass substrates caused by contact with several plates.
KITABAYASHI HIROYOSHI (1); FUJII HARUHISA (1); OISHI TAKAYUKI (2); HONDA KATSUHIKO (2)
(1) Mitsubishi Electric Corp.; (2) ADI
Seidenki Gakkai Koen Ronbunshu, 1997, VOL.1997, PAGE.297-298, FIG.2, REF.3
JOURNAL NUMBER: F0983BAO ISSN NO: 1342-1492
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication

ABSTRACT: Recently, in the fabrication of TFT-**LCD**, contact electrification of glass substrate with plates in separation process is probable to cause the ESD problem to the devices. We measured the charging potential of glass substrate by using electrostatic voltmeter when the glass substrate was separated from a **dielectric**-coated plate. From the experiment, we obtained the following results. The contact charging potential of glass substrate depended on the number of contact and the plate material. (author abst.)

32/3,AB/32 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02385621 JICST ACCESSION NUMBER: 95A0505910 FILE SEGMENT: JICST-E
Liquid crystal displays.
KASHIMOTO MIYUKI (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1995, VOL.13,NO.35, PAGE.85-91, FIG.4
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

32/3,AB/33 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02291453 JICST ACCESSION NUMBER: 95A0021185 FILE SEGMENT: JICST-E
1995 latest **liquid crystal** process technology. Etching technology. Dry etching equipment. CLR-7000 Plasma-Therm.
Gekkan Semiconductor World(Semiconductor World), 1994, VOL.13,NO.13, PAGE.82, FIG.2
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The CLR-7000 is a dry etching device which has a high-performance plasma treatment room to produce FPD for large areas to the size of 500*500mm. Applicable substances in terms of etching purposes are a-Si, **SiN** and **SiO** as **insulating** films and Al, Cr, Mo, Ta and ITO as metallic thin films. The largest capacity of processing is 60 panels/h. The PECVD type of the CLR-7000 will be released in the middle of 1995.

32/3,AB/34 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01765274 JICST ACCESSION NUMBER: 93A0492730 FILE SEGMENT: JICST-E
a-Si TFTs with Stacked Gate Isulator of CVD-**SiO2**/PECVD-SiNx.
FUKUDA KAICHI (1); IBARAKI NOBUKI (1)
(1) Toshiba Corp., Electron Device Engineering Lab.
Denshi Joho Tsushin Gakkai Ronbunshi. C,2(Transactions of the Institute of Electronics, Information and Communication Engineers. C-2), 1993,

VOL.76,NO.5, PAGE.184-191, FIG.12, REF.10
JOURNAL NUMBER: L0196AAD ISSN NO: 0915-1907
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

32/3,AB/35 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01125984 JICST ACCESSION NUMBER: 90A0911669 FILE SEGMENT: JICST-E
Effect of gate **insulator** on amorphous silicon thin film transistor performance.
SOUK J H (1); BATEY J (1); PARSONS G N (1); LIBSCH F R (1)
(1) IBM Research Division, NY
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1990, VOL.90,NO.288(EID90 64-73), PAGE.17-22, FIG.6, TBL.3, REF.7
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397 621.382.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Amorphous silicon (a-Si) thin film transistors (TFTs) have become the dominat technology for driving active metrix **liquid crystal** displays. Gate **insulator** quality is one of the most important issues in determining TFT performance. We have performed a detailed study on various **insulators** used in amorphous silicon TFT displays. Properties of various PECVD silicon nitrides and **silicon dioxide** will be discussed based on electrical and mechanical measurements and with regrad to their influence on TFT processing and performance. Transistors fabricated with various **insulators** were characterized by measuring mobility, threshold voltage and transfer characteristics. TFTs with optimum gate dielectrics have been fabricated with threshold voltage .IMAGE. 2.0 V, field-effect mobility > 1.0cm2/vs and ON/OFF ratio of over 107. (author abst.)

32/3,AB/36 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

01268766 ERA-08-051700; EDB-83-168769
Title: Reports of the research laboratory, Asahi Glass Co., Ltd. Volume 32, Number 1, 1982
Corporate Source: Asahi Glass Co. Ltd., Yokohama (Japan). Research Lab.
Publication Date: 1982
p 73
Report Number(s): PB-83-209965
Language: English
Abstract: This issue contains six reports from the Research Laboratory. All reports have an English Abstract with English text as noted. The contents are: Mechanical properties of **silica** films evaporated on Columbia Resin CR-39 (Japanese); Improvement of **LCD** legibility for automobiles (English); Strength distribution of sintered **silicon nitride** (English); Zirconia fusion cast refractory

(Japanese); The determination of very small amount of tin in lead glass by atomic absorption spectrometry (Japanese); Polyphenylene sulfide for electrical **insulation** use (Japanese).

33/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6402499 INSPEC Abstract Number: B1999-12-0520F-096
Title: Advanced PECVD technology for manufacturing AM LCDs
Author(s): Chuang-Chuang Tsai; Quanyuan Shang; Takehara, T.; Harshbarger, W.; Law, K.
Author Affiliation: Appl. Komatsu Technol., Santa Clara, CA, USA
Conference Title: Proceedings of 5th Asian Symposium on Information Display. ASID '99 (IEEE Cat. No.99EX291) p.267-71
Editor(s): Wu, I-W; Shieh, H.-P.
Publisher: SID Taipei Chapter, Taipei, Taiwan
Publication Date: 1999 Country of Publication: Taiwan xvi+368 pp.
ISBN: 957 97347 9 8 Material Identity Number: XX-1999-00988
Conference Title: Proceedings of the 5th Asian Symposium on Information Display. ASID'99
Conference Sponsor: SID Asian Regions (SID Beijing, Hong Kong, Japan & Korea Chapters); IEICE, ITE Nat. Sci. Council, Taiwan; Taiwan FPD Forum; Minstr. Econ. Affairs/Dept. Ind. Technol.; IEEE Electron. Devices Soc
Conference Date: 17-19 March 1999 Conference Location: Hsinchu, Taiwan
Language: English
Abstract: PECVD is one of the most critical technologies for manufacturing AM **LCD** devices. Advanced PECVD systems have been developed for low temperature deposition of a-Si, **SiN**/sub x/, **SiO** /sub 2/, SiON, and n-Si films. Typically, cluster tool configurations are used since they provide excellent process control with single substrate processing and flexible process flows. Recent reports indicate that good polysilicon TFTs have been manufactured using laser crystallization of a-Si precursor films. This paper reviews the development of PECVD systems for volume manufacturing of LCDs and discusses process technology and requirements for future manufacturing.
Subfile: B

33/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5926179 INSPEC Abstract Number: B9807-7260-038
Title: Studies of rf-sputtered CrSiO/sub x/ and SiC as series resistor films in FEDs
Author(s): Nowicki, R.S.; Busta, H.H.; Pogemiller, J.E.; Forouhi, A.R.; Bloomer, I.; Clift, W.M.; Yio, J.L.; Felter, T.
Author Affiliation: Coloray Display Corp., Fremont, CA, USA
Conference Title: 1996 SID International Symposium. Digest of Technical Papers. First Edition p.456-8
Publisher: Soc. Inf. Display, Santa Ana, CA, USA
Publication Date: 1996 Country of Publication: USA xx+1022 pp.
Material Identity Number: XX96-00687
Conference Title: Proceedings of SID '96
Conference Date: 12-17 May 1996 Conference Location: San Diego, CA, USA
Language: English
Abstract: We have studied the physical and electrical properties of Cr-**SiO** /sub x/ ("cermet") and SiC films for use as series resistors in field emitter displays (FEDs). The cermet films were RF reactively sputtered from a CrSi/sub 2/ target in an oxygen/argon mixture. For cermet, we find that as-deposited films are amorphous and exhibit high-Mohm-cm

resistivity with refractive index values approaching that of **silicon nitride**, whereas films heat treated at 350 degrees C for ca. one hour in air or under vacuum are loosely crystalline and exhibit low-to-mid-10E+4 ohm-cm resistivity and refractive index values approaching that of **SiO** /sub 2/. The crystallized films exhibit a roughened surface which will generate microdefects in an overlying oxide film. For sputtered SiC, the as-deposited films are amorphous, with resistivity values of high-10E+4 ohm-cm. The heat created SiC films are finely crystalline, with resistivity values of low-to-mid-10E+5 ohm-cm. They also exhibit the desirable near-linear ohmic characteristics.
Subfile: B

33/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5684444 INSPEC Abstract Number: B9710-2120-010
Title: Studies of RF sputtered CrSiOx and SiC as series resistor films in FED displays
Author(s): Nowicki, RS.; Busta, H.H.; Pogemiller, J.E.; Forouhi, A.R.; Bloomer, I.; Clift, W.M.; Ja Lee Yio; Felter, T.
Author Affiliation: Coloray Display Corp., Fremont, CA, USA
Conference Title: IVMC'96. 9th International Vacuum Microelectronics Conference. Technical Digest. (Cat. No.96TH8212) p.184-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA xvi+703 pp.
ISBN: 0 7803 3594 5 Material Identity Number: XX97-01456
Conference Title: 9th International Vacuum Microelectronics Conference
Conference Sponsor: Russian Fund of Basic Res.; Russian Minist. Sci.; St. Petersburg City Adm. & City Legislative Assembly; U.S. Adv. Res. Projects Agency (ARPA); Eur. Res. Office of the U.S. Army; Eur. Office of Aerosp. Res. & Dev., U.S. Air Force; U.S. Office of Naval Res. - Eur
Conference Date: 7-12 July 1996 Conference Location: St. Petersburg, Russia
Language: English
Abstract: We have studied the physical and electrical properties of Cr-SiOx ("cermet") and SiC films for use as series resistors in field emitter displays (FEDs). The cermet films were RF reactively sputtered from a CrSi/sub 2/ target in an oxygen/argon mixture. For cermet, we find that as-deposited films are amorphous and exhibit high-Mohm-cm resistivity with refractive index values approaching that of **silicon nitride**, whereas films heat treated at 350 degrees C for ca. one hour in air or under vacuum are loosely crystalline and exhibit low-to-mid-10E+4 ohm-cm resistivity and refractive index values approaching that of **SiO**/sub 2/. The crystallized films exhibit a roughened surface which will generate microdefects in an overlying oxide film. For sputtered SiC, the as-deposited films are amorphous, with resistivity values of high-10E+4 ohm cm. The heat treated SiC films are finely crystalline, with resistivity values of low-to-mid-10E+5 ohm-cm. They also exhibit the desirable near-linear ohmic characteristics.
Subfile: B

33/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5475285 INSPEC Abstract Number: B9702-2560R-075

03/25/2003

Title: Effects of NH/sub 3/ plasma passivation on N-channel polycrystalline silicon thin-film transistors
Author(s): Huang-Chung Cheng; Fang-Shing Wang; Chun-Yao Huang
Author Affiliation: Dept. of Electron. Eng., Nat. Chiao Tung Univ., Hsinchu, Taiwan
Journal: IEEE Transactions on Electron Devices vol.44, no.1 p.64-8
Publisher: IEEE,
Publication Date: Jan. 1997 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(199701)44:1L.64:EPPC;1-8
Material Identity Number: I037-97001
U.S. Copyright Clearance Center Code: 0018-9383/97/$10.00
Language: English
Abstract: The NH/sub 3/-plasma passivation has been performed on polycrystalline silicon (poly-Si) thin-film transistors (TFT's), It is found that the TFT's after the NH/sub 3/-plasma passivation achieve better device performance, including the off-current below 0.1 pA/ mu m and the on/off current ratio higher than 10/sup 8/, and also better hot-carrier reliability than the H/sub 2/-plasma devices. Based on optical emission spectroscopy (OES) and secondary ion mass spectroscopy (SIMS) analysis, these improvements were attributed to not only the hydrogen passivation of the defect states, but also the nitrogen pile-up at **SiO** /sub 2//poly-Si interface and the strong **Si-N** bond formation to terminate the dangling bonds at the grain boundaries of the polysilicon films. Furthermore, the gate-oxide leakage current significantly decreases and the oxide breakdown voltage slightly increases after applying NH/sub 3/-plasma treatment. This novel process is of potential use for the fabrication of TFT/**LCD**'s and TFT/SRAM's.
Subfile: B

33/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

4430253 INSPEC Abstract Number: A9315-6130-013
Title: Azimuthal anchoring energy at a **SiO**/sub x/-nematic interface
Author(s): Nobili, M.; Lazzari, C.; Schirone, A.; Faetti, S.
Author Affiliation: Dipartimento di Fisica, Pisa Univ., Italy
Journal: Molecular Crystals and Liquid Crystals vol.212 p.97-106
Publication Date: Feb. 1992 Country of Publication: UK
CODEN: MCLCA5 ISSN: 0026-8941
Language: English
Abstract: The azimuthal anchoring energy at the interface between the nematic **liquid crystal** pentylcyanobiphenyl (5CB) and an obliquely evaporated **SiO** /sub x/ substrate is measured by using a reflectometric method. The time response of the director at the surface is investigated and two very different regimes are evidenced. The azimuthal anchoring energy coefficient exhibits an almost-critical behaviour near the clearing temperature and is almost independent on the thickness d of the **SiO** /sub x/ layer but it exhibits a sharp decrease of d<or=d/sub c/ approximately=25 AA. The anchoring function is found to depend on the azimuthal director angle phi as W(phi)=W/sub a//2 **sin**/sup 2/(phi).
Subfile: A

33/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03940833 INSPEC Abstract Number: A91102637
Title: Experimental measurement of the azimuthal anchoring energy function at a **SiO**-nematic interface
Author(s): Faetti, S.; Nobili, M.; Schirone, A.
Author Affiliation: Dipartimento di Fisica, Pisa Univ., Italy
Journal: Liquid Crystals vol.10, no.1 p.95-100
Publication Date: July 1991 Country of Publication: UK
CODEN: LICRE6 ISSN: 0267-8292
Language: English
Abstract: The functional form of the azimuthal anchoring energy, i.e., the anisotropic part of the interfacial free energy, at the interface between the nematic **liquid crystal** 4-n-pentyl-4'-cyanobiphenyl and an obliquely evaporated **SiO** substrate is measured for the first time by using a reflectometric method. The anchoring energy function is obtained by measuring the director rotation on the interface caused by an external magnetic field ranging from 0 to 2.3 T. The dependence of the anchoring energy on the director azimuthal angle is found to be well fitted by the function W/sub a/(phi)=W/sub a/**sin**/sup 2/ phi in agreement with the predictions of the Berreman model for the anchoring at a grooved interface.
Subfile: A

33/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

03567552 INSPEC Abstract Number: B90018661
Title: Thin film transistors for addressing LC-flat panel displays
Author(s): Kallfass, T.
Author Affiliation: Inst. fuer Netzwerk- und Systemtheorie, Stuttgart Univ., West Germany
Conference Title: Proceedings. VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks (Cat. No.89CH2704-5) p.2/20-23
Publisher: IEEE Comput. Soc. Press, Washington, DC, USA
Publication Date: 1989 Country of Publication: USA xiv+791 pp.
ISBN: 0 8186 1940 6
U.S. Copyright Clearance Center Code: CH2704-5/89/0000-2020$01.00
Conference Sponsor: IEEE; Gesellschaft fur Inf.; Verband Deutscher Elektrotech
Conference Date: 8-12 May 1989 Conference Location: Hamburg, West Germany
Language: English
Abstract: Thin-film transistors (TFTs) are exceptionally qualified for addressing large-area **liquid-crystal** displays. The TFT circuits and the requirements for operating the picture elements in the displays are described. Further comments focus on the staggered structure of the TFTs and the materials a-Si:H and poly-CdSe used as semiconductors and Ta/sub 2/O/sub 5/, **SiO**/sub 2/, and **SiN** for gate isolators. The electrical data (such as mobility and off-current) of the TFTs determine the optical performance of the displays, characterized by a high contrast and a wide viewing angle.
Subfile: B

33/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

• 03/25/2003

02505983 INSPEC Abstract Number: A85095534
Title: A novel method for determining the anchoring energy function at a nematic **liquid crystal**-wall interface from director distortions at high fields
Author(s): Yokoyama, H.; van Sprang, H.A.
Author Affiliation: Electrotech. Lab., Ibaraki, Japan
Journal: Journal of Applied Physics vol.57, no.10 p.4520-6
Publication Date: 15 May 1985 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/85/104520-07$02.40
Language: English
Abstract: The anchoring energy function, i.e. the anisotropic part of the interfacial free energy, at a nematic **liquid crystal**-wall interface can be determined uniquely without a numerical fitting procedure, when the integrated birefringence of a **liquid crystal** cell with a thickness much larger than the extrapolation length is measured as a function of an electric or magnetic field well above the Freedericksz threshold. The precision of the method is closely argued, showing that the resulting anchoring energy function is reasonably insensitive to the uncertainties in the material parameters and in the cell thickness. As an example, the anchoring energy function at the interface between 5CB(pentylcyanobiphenyl) and obliquely evaporated **SiO** was determined for the first time, by measuring the birefringence and the capacitance of a 56- mu m-thick cell up to 150 V rms at 0.23 degrees C below the clearing temperature. A saturation of the field-induced distortion was clearly observed at about 100 V rms. The anchoring energy function was found to be well fitted by a function of the form /sup 1///sub 2/E/sub a/ **sin**/sup 2/ theta +/sup 1///sub 4/E/sub 1/ **sin**/sup 4/ theta , where theta is the angle between the boundary director and the substrate, with E/sub a/ approximately 4.0*10/sup -5/ J/m/sup 2/ and E/sub 1/ approximately -1.8*10/sup -5/ J/m/sup 2/.
Subfile: A

33/3,AB/9 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04605031
E.I. No: EIP97013508108
Title: Effects of NH//3 plasma passivation on N-channel polycrystalline silicon thin-film transistors
Author: Cheng, Huang-Chung; Wang, Fang-Shing; Huang, Chun-Yao
Corporate Source: Natl Chiao Tung Univ, Hsinchu, Taiwan
Source: IEEE Transactions on Electron Devices v 44 n 1 Jan 1997. p 64-68
Publication Year: 1997
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: The NH//3-plasma passivation has been performed on polycrystalline silicon (poly-Si) thin-film transistors (TFT's). It is found that the TFT's after the NH//3-plasma passivation achieve better device performance, including the off-current below 0.1 pA/ mu m and the on/off current ratio higher than 10**8, and also better hot-carrier reliability than the H//2-plasma ones. Based on optical emission spectroscopy (OES) and secondary ion mass spectroscopy (SIMS) analysis, these improvements were attributed to not only the hydrogen passivation of the defect states, but also the nitrogen pile-up at **SiO**//2/poly-Si interface and the strong **Si-N** bond formation to terminate the dangling bonds at the grain boundaries of the polysilicon films. Furthermore, the gate-oxide leakage current significantly decreases and the oxide breakdown voltage slightly increases after applying NH//3-plasma

treatment. This novel process is of potential use for the fabrication of TFT/**LCD**'s and TFT/SRAM's. (Author abstract) 19 Refs.

33/3,AB/10 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08259862 Genuine Article#: 253FE Number of References: 24
Title: Electrospray ionization mass spectrometry and on-line capillary zone electrophoresis - mass spectrometry for the characterization of citrate synthase (ABSTRACT AVAILABLE)
Author(s): McComb ME; Donald LJ; Perreault H (REPRINT)
Corporate Source: UNIV MANITOBA,DEPT CHEM/WINNIPEG/MB R3T 2N2/CANADA/ (REPRINT); UNIV MANITOBA,DEPT CHEM/WINNIPEG/MB R3T 2N2/CANADA/
Journal: CANADIAN JOURNAL OF CHEMISTRY-REVUE CANADIENNE DE CHIMIE, 1999, V 77, N11 (NOV), P1752-1760
ISSN: 0008-4042 Publication date: 19991100
Publisher: NATL RESEARCH COUNCIL CANADA, RESEARCH JOURNALS, MONTREAL RD, OTTAWA ON K1A 0R6, CANADA
Language: English Document Type: ARTICLE
Abstract: The enzyme citrate synthase from E. coli is a protein with a molecular weight (M-r) of 47 885 Da (wild type). This enzyme has been studied extensively, and its amino acid sequence has been characterized. This model protein has been used in this work for development and validation of methods involving capillary electrophoresis (CE) and electrospray ionization mass spectrometry (ESI-MS). The nti, determinations were conducted using sample infusion ESI-MS, and the tryptic digestion products of wild-type citrate synthase were characterized by on-line CE-ESI-MS coupled with a sheathless interface. On-line experiments were conducted on two different mass spectrometers, a Quattro-LC triple quadrupole instrument equipped with a Z-Spray(TM) source (Micromass), and a reflecting time-of-flight (TOF) mass spectrometer builtin-house in the Time-of-Flight Laboratory, Department of Physics, University of Manitoba. This is the first article to be written on the interfacing of a Z-Spray(TM) source with CE. Unmodified fused **silica** capillaries gold-coated sheathless interfaces were used. The an-line CE separations yielded theoretical plate numbers greater than 10(4) on average. Selected ion erectrophorograms (SIE) of the tryptic peptides recorded on the Quattro-**LC displayed SIN** ratios ranging from ca. 14 to 120 on raw data. These SIE enabled identification of each peptide. The use of reflecting time-of-flight mass spectrometry (TOFMS) afforded mass resolution values of ca. 6000 (m/Delta m(FWHM)), which enabled isotopic resolution of the peptide components. CE-ESI-MS and CE-ESI-TOFMS experiments enabled the generation of a complete tryptic map of citrate synthase.

33/3,AB/11 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02452239 Genuine Article#: LB960 Number of References: 254
Title: CHEMICAL ASPECTS OF SOLUTION ROUTES TO PEROVSKITE-PHASE MIXED-METAL OXIDES FROM METAL-ORGANIC PRECURSORS
Author(s): CHANDLER CD; ROGER C; HAMPDENSMITH MJ
Corporate Source: UNIV NEW MEXICO,DEPT CHEM/ALBUQUERQUE//NM/87131; UNIV NEW MEXICO,DEPT CHEM/ALBUQUERQUE//NM/87131; UNIV NEW MEXICO,CTR MICROENGN CERAM/ALBUQUERQUE//NM/87131
Journal: CHEMICAL REVIEWS, 1993, V93, N3 (MAY), P1205-1241

ISSN: 0009-2665
Language: ENGLISH Document Type: REVIEW

33/3,AB/12 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01415639 Genuine Article#: GX228 Number of References: 7
Title: HIGH-STABILITY METAL A-SIN0.5-H METAL DIODE FOR **LCD** APPLICATION (Abstract Available)
Author(s): YOSHIDA K; UCHIDA H; MIZOBATA E; HIRAI Y; KANEKO S
Corporate Source: NEC CORP LTD,FUNCT DEVICES RES LABS,4-1-1 MIYAZAKI,MIYAMAE KU/KAWASAKI/KANAGAWA 216/JAPAN/
Journal: JOURNAL OF NON-CRYSTALLINE SOLIDS, 1991, V137, DEC (DEC), P 1287-1290
Language: ENGLISH Document Type: ARTICLE
Abstract: We have investigated instability in metal/ a-SiN0.5:H/ metal diodes and successfully produced a highly stable diode. Instability is produced by the decrease in current encountered during voltage application. This decrease is caused by a change in dangling bond density, which may itself by the bonding instability of silicon or hydrogen. We have been able to improve diode stability, while still maintaining high nonlinearity, by annealing at 500-degrees-C for 1 hour in an N2 atmosphere. This annealing may have had the effect of effusing hydrogen atoms, and either breaking or correcting bonds whose instability is caused by deviations from the norm in their lengths or angles.

33/3,AB/13 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05212636 JICST ACCESSION NUMBER: 02A0659927 FILE SEGMENT: JICST-E
Growth Mode of Polycrystalline-Si Prepared by Excimer Laser Annealing. Relationship between the Grain Morphology and Hydrogens.
KAWAMOTO NAOYA (1); MATSUO NAOTO (1); ABE HISASHI (2); MIYAI YOSHIO (2); HAMADA HIROKI (2)
(1) Yamaguchi Univ., Fac. of Eng.; (2) Sanyo Electric Co., Ltd.
Denshi Joho Tsushin Gakkai Ronbunshi C(Transactions of the Institute of Electronics, Information and Communication Engineers C), 2002, VOL.J85-C,NO.8, PAGE.659-665, FIG.12, REF.10
JOURNAL NUMBER: S0623CAH ISSN NO: 1345-2827
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Here was investigated a polycrystalline silicon (poly-Si) recrystallized an amorphous silicon (a-Si) depositted by using PECVD (plasma enhanced chemical vapor deposition) onto a substrate with a structure of **SiN**/**SiO2**/glass by using excimer laser annealing (ELA) method. On comparing a-Si depositted onto a quartz substrate by using low-pressure chemical vapor deposition (LPCVD) method with poly-Si obtained by using ELA, poly-Si on **SiN** substrate has larger Raman intensity and smaller inner stress working in a crystal. Avearage diameter of poly-Si on the **SiN** substrate was 70 nm, but could observe no disc-like grains ovservable at poly-Si on a quartz substrate. And, on surface roughness, surface of poly-Si on the **SiN** substrate was larger than that of poly-Si on the quartz

substrate, too. These test results are thought to be based on defference of crystal growth mechanism between poly-Sis formed on **SiN** and quartz substrates, so on the mechanism some investigations on hydrogen in the film and from a viewpoint of its origin were carried out.

33/3,AB/14 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03219826 JICST ACCESSION NUMBER: 97A0516157 FILE SEGMENT: JICST-E
Light shielding films and their forming methods.
SHIMIZU TOSHIO (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1997, VOL.15,NO.28, PAGE.75-76, FIG.1
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

33/3,AB/15 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02592994 JICST ACCESSION NUMBER: 95A0624744 FILE SEGMENT: JICST-E
Glass substrate for **liquid crystal** displays.
TAKEMURA MOTOKO (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1995, VOL.13,NO.46, PAGE.181-182, FIG.1
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

33/3,AB/16 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02291457 JICST ACCESSION NUMBER: 95A0021189 FILE SEGMENT: JICST-E
1995 latest **liquid crystal** process technology. Film formation technology - CVD.Plasma CVD equipment. PD-4800.Samco International Laboratory.
Gekkan Semiconductor World(Semiconductor World), 1994, VOL.13,NO.13, PAGE.91, FIG.1, TBL.1
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The PD-4800 is a full-automatic, large plasma CVD system for mass production of thin films up to the size A4, such as a-Si films, Si nitride films and Si oxide films. Characteristic points of this product are as follows : The shower electrode structure to realize excellent

uniformity of the film. A structure to prevent flakes from generating. Full-automatic operation under a programmable controller. Various interlocking mechanisms.

33/3,AB/17 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02291446 JICST ACCESSION NUMBER: 95A0021178 FILE SEGMENT: JICST-E
1995 latest **liquid crystal** process technology. Etching technology. RIE equipment. RIE-4800.Samco International Laboratory.
Gekkan Semiconductor World(Semiconductor World), 1994, VOL.13,NO.13, PAGE.75, FIG.1, TBL.1
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: RIE-4800 is the full-automatic, large reactive ion etching equipment to meet up to the A4 size. A standard model is equipped with a safety mechanism using an interlock, and it accepts various monitors. This type of equipment enables us to obtain etching patterns with little side-etching for Si or Al thin films and high etch selectivity.

33/3,AB/18 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01192751 JICST ACCESSION NUMBER: 91A0180576 FILE SEGMENT: JICST-E
Low-temperature polysilicon thin film transistors by non-mass-separated ion flux doping technique.
MASUMO K (1); KUNIGITA M (1); TAKAFUJI S (1); NAKAMURA N (1); IWASAKI A (1); YUKI M (1)
(1) Asahi Glass Co., Ltd., Yokohama
Jpn J Appl Phys Part 2, 1990, VOL.29,NO.12, PAGE.L2377-L2379, FIG.8, REF.15
JOURNAL NUMBER: F0599BAD ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS 621.382.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: A low-temperature, high-throughput self-aligned poly-Si TFT fabrication process has been developed. The process includes two key techniques. The first one is a laser-induced crystallization of a-Si occurring in the solid phase using a CW Ar+ laser beam with high scanning speed, which was previously reported. The second is large-diameter ion flux doping without mass separation. The maximum processing temperature is 450.DEG.C., which is sufficiently low for use of inexpensive glass substrates. With this process, excellent poly-Si TFT characteristics of Ion/Ioff>106 and .MU.FE=40cm2/(Vvs) were obtained. (author abst.)

33/3,AB/19 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15015644 PASCAL No.: 01-0172238

03/25/2003

Effects of Backgate Voltage on Electrical Characteristics of Poly-Si Thin Film Transistors Fabricated on Stainless-Steel Substrate

SERIKAWA Tadashi; OMATA Fujio
NTT Cyber Space Laboratories, 3-9-11 Midori-cho, Musashino, Tokyo 180-0012, Japan

Journal: Japanese Journal of Applied Physics Part II : Letters, 2000-12-15, 39 (12B) L1277-L1279
Language: English

High mobility p-channel polycrystalline Si thin film transistors (poly-Si TFTs) are fabricated on flexible stainless-steel substrates coated with 500-nm-thick **SiO2** and 50-nm-thick **SiN** films. The electrical characteristics of mobility, threshold voltage and subthreshold slope are first measured as a function of backgate voltage V SUB B SUB G of from -26 V to +20 V applied on stainless-steel substrate. Mobilities show small dependence on V SUB B SUB G . Threshold voltages, however, have dependence of decreasing with increasing V SUB B SUB G . Subthreshold slopes also show concave-shaped dependence on V SUB B SUB G . The results indicate that electrical characteristics of poly-Si TFTs are controlled by simply applying voltages to the substrate. Thus, application of backgate voltage are very important for design advanced poly-Si TFT integrated circuits and to secure stable operation of the circuits.

33/3,AB/20 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

12860919 PASCAL No.: 97-0119615

Effects of NH SUB 3 plasma passivation on N-channel polycrystalline silicon thin-film transistors

CHENG H C; WANG F S; HUANG C Y
Natl Chiao Tung Univ, Hsinchu, Taiwan

Journal: IEEE Transactions on Electron Devices, 1997, 44 (1) 64-68
Language: English

The NH SUB 3 -plasma passivation has been performed on polycrystalline silicon (poly-Si) thin-film transistors (TFT's). It is found that the TFT's after the NH SUB 3 -plasma passivation achieve better device performance, including the off-current below 0.1 pA/ mu m and the on/off current ratio higher than 10 SUP 8 , and also better hot-carrier reliability than the H SUB 2 -plasma ones. Based on optical emission spectroscopy (OES) and secondary ion mass spectroscopy (SIMS) analysis, these improvements were attributed to not only the hydrogen passivation of the defect states, but also the nitrogen pile-up at **SiO** SUB 2 /poly-Si interface and the strong **Si-N** bond formation to terminate the dangling bonds at the grain boundaries of the polysilicon films. Furthermore, the gate-oxide leakage current significantly decreases and the oxide breakdown voltage slightly increases after applying NH SUB 3 -plasma treatment. This novel process is of potential use for the fabrication of TFT/**LCD**'s and TFT/SRAM's.

35/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7440348 INSPEC Abstract Number: B2002-12-7260B-031
Title: Low temperature amorphous and nanocrystalline silicon technology for flat panel displays
Author(s): Wagner, S.; Gleskova, H.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Conference Title: Conference Record of the 20th International Display Research Conference p.402-5
Publisher: Soc. Inf. Display, San Jose, CA, USA
Publication Date: 2000 Country of Publication: USA xviii+454 pp.
Material Identity Number: XX-2002-02434
Conference Title: Conference Record of the 20th International Display Research Conference
Conference Sponsor: Soc. Inf. Display; IEEE Electron Devices Soc
Conference Date: 25-28 Sept. 2000 Conference Location: Palm Beach, FL, USA
Language: English
Abstract: Silicon thin film transistor processes for active **matrix** backplanes can be adapted to organic polymer substrates. The criteria initially most important for substrate selection are thermal compatibility with the transistor process and bonding with the first deposited layer. Candidate transistor technologies include hydrogenated amorphous silicon (a-Si:H) and nanocrystalline silicon (nc-Si:H). We describe amorphous silicon transistors on polyimide foil using a **silicon nitride** gate **dielectric** optimized for 150 degrees C. These transistors perform almost as well as those made by conventional processing on glass.
Subfile: B

35/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6910784 INSPEC Abstract Number: A2001-11-8115H-022, B2001-06-0520F-021
Title: Low temperature growth of **silicon nitride** by electron cyclotron resonance plasma enhanced chemical vapour deposition
Author(s): Flewitt, A.J.; Dyson, A.P.; Robertson, J.; Milne, W.I.
Author Affiliation: Dept. of Eng., Cambridge Univ., UK
Journal: Thin Solid Films Conference Title: Thin Solid Films (Switzerland) vol.383, no.1-2 p.172-7
Publisher: Elsevier,
Publication Date: 15 Feb. 2001 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(20010215)383:1/2L.172:TGSN;1-O
Material Identity Number: T070-2001-007
U.S. Copyright Clearance Center Code: 0040-6090/2001/$20.00
Conference Title: Third Symposium on Thin Films for Large Area Electronics
Conference Date: 30 May-2 June 2000 Conference Location: Strasbourg, France
Language: English
Abstract: **Silicon nitride** (a-**SiN**) is extensively used as the gate **insulator** layer in thin films transistors (TFTs) for active **matrix liquid crystal** displays. Such displays are currently produced on thin, glass substrates; plastic substrates offer a cheaper and more robust alternative, but have maximum process temperatures

below 150 degrees C. The deposition of a-**SiN** by rf plasma enhanced chemical vapour deposition (PECVD) requires the production of **SiN**/sub x/H/sub y/ radicals in the plasma. However, as N/sub 2/ is very stable, a gas mixture of SiH/sub 4/ with NH/sub 3/ is required for this to take place, which yields a hydrogen-rich material. High substrate temperatures (~300 degrees C) are therefore required to drive out the excess hydrogen. In electron cyclotron resonance (ECR)-PECVD, a highly ionised plasma (~10/sup 16/ m/sup -3/) with very low ion energies (~10 eV) can be produced. This allows the dissociation of N/sub 2/ into atomic N, and hence a gas phase reaction can take place directly with SiH/sub 4/, which results in a material with a lower hydrogen content than is obtained with NH/sub 3/ gas. Energy for further H removal is provided by the bombardment of He ions, allowing a reduction in the deposition temperature to 80 degrees C. In this way a-**SiN** has been produced with a resistivity of 3*10/sup 14/ Omega cm and an average breakdown strength of 4.5 MV cm/sup -1/.
Subfile: A B

35/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6761663 INSPEC Abstract Number: B2000-12-2560R-118
Title: A high-voltage hydrogenated amorphous silicon thin-film transistor for reflective active-**matrix** cholesteric **LCD**
Author(s): Nahm, J.Y.; Kanicki, J.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Conference Title: Flat-Panel Displays and Sensors - Principles, Materials and Processes. Symposium (Materials Research Society Symposium Proceedings Vol.558) p.125-8
Editor(s): Chalamala, B.R.; Friend, R.H.; Jackson, T.N.; Libsch, F.R.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 2000 Country of Publication: USA xv+615 pp.
ISBN: 1 55899 465 3 Material Identity Number: XX-2000-01520
Conference Title: Flat-Panel Displays and Sensors - Principles, Materials and Processes. Symposium
Conference Date: 4-9 April 1999 Conference Location: San Francisco, CA, USA
Language: English
Abstract: A high-voltage hydrogenated amorphous silicon thin film transistor (HV a-Si:H TFT) with thick double layer gate **insulator** (~0.95 mu m) has been developed for reflective active-**matrix** cholesteric **liquid crystal** displays. The double layer gate **insulator** consists of 0.85 and 0.10 mu m thick benzocyclobutene and hydrogenated amorphous **silicon nitride**, respectively. This HV a-Si:H TFT operates at the gate-to-source and drain-to-source biases up to 100 V without any serious leakage current degradation and device breakdown.
Subfile: B

35/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6525239 INSPEC Abstract Number: B2000-04-2560R-118
Title: An amorphous silicon thin-film transistor with fully self-aligned top gate structure
Author(s): Powell, M.J.; Glasse, C.; Green, P.W.; French, I.D.; Stemp,

I.J.
Author Affiliation: Philips Res. Lab., Redhill, UK
Journal: IEEE Electron Device Letters vol.21, no.3 p.104-6
Publisher: IEEE,
Publication Date: March 2000 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200003)21:3L.104:ASTF;1-8
Material Identity Number: I338-2000-003
U.S. Copyright Clearance Center Code: 0741-3106/2000/$10.00
Language: English
Abstract: We have developed a novel fully self-aligned top gate amorphous silicon thin-film transistor, which shows excellent transistor characteristics. Self-alignment is achieved by patterning the gate electrode and then etching the **silicon nitride** gate **insulator** , followed by silicidation and ion implantation of the exposed a-Si in the contact regions. We obtain a long channel saturated mobility of 0.9 cm/sup 2/ V/sup -1/ s/sup -1/, while for channel lengths of 6 mu m, we obtain an effective mobility of 0.6 cm/sup 2/ V/sup -1/ s/sup -1/, in the saturated region and 0.5 cm/sup 2/ V/sup -1/ s/sup -1/, in the linear region. This high level of performance, together with the negligible parasitic capacitance of the self-aligned structure, makes this transistor suitable for new demanding applications in active **matrix liquid crystal** displays and large area X-ray image sensors.
Subfile: B

35/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6324797 INSPEC Abstract Number: B1999-09-7260F-020
Title: Damascene-gate thin film transistors with ultra-thin gate dielectrics
Author(s): Ma, E.Y.; Wagner, S.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Conference Title: Conference Proceedings. LEOS'98. 11th Annual Meeting. IEEE Lasers and Electro-Optics Society 1998 Annual Meeting (Cat. No.98CH36243) Part vol.1 p.132-3 vol.1
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1998 Country of Publication: USA 2 vol.(xvi+48+xviii+449) pp.
ISBN: 0 7803 4947 4 Material Identity Number: XX-1998-03666
U.S. Copyright Clearance Center Code: 0 7803 4947 4/98/$10.00
Conference Title: Conference Proceedings. LEOS'98. 11th Annual Meeting. IEEE Lasers and Electro-Optics Society 1998 Annual Meeting
Conference Date: 1-4 Dec. 1998 Conference Location: Orlando, FL, USA
Language: English
Abstract: Summary form only given. The push towards larger and higher resolution flat panel displays requires an improvement in current thin-film transistor (TFT) performance. Devices should have lower threshold voltages, sub-threshold slopes and, in particular, lower gate line resistances if large, high-resolution, video quality displays are to be realized. This can be achieved by using thicker gate lines and thinner gate dielectrics. However, since amorphous silicon TFTs currently being used in active-**matrix liquid crystal** displays are bottom-gate structures, there is the problem of step coverage. Specifically, a thick gate **dielectric** is required to adequately cover the gate metal in order to prevent leakage current between the gate and the source/drain. The approach presented in this paper is to embed the gate metal into a trench made into a **silicon nitride** passivating layer above the

substrate so that the top of the gate metal is level with the surface of the passivating layer. This damascene-gate structure has several advantages.
Subfile: B

35/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6206029 INSPEC Abstract Number: B1999-05-2560R-018
Title: Planarized copper gate hydrogenated amorphous-silicon thin-film transistors for AM-LCDs
Author(s): Je-Hsiung Lan; Kanicki, J.
Author Affiliation: Center for Display Technol. & Manuf., Michigan Univ., Ann Arbor, MI, USA
Journal: IEEE Electron Device Letters vol.20, no.3 p.129-31
Publisher: IEEE,
Publication Date: March 1999 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199903)20:3L.129:PCGH;1-C
Material Identity Number: I338-1999-003
U.S. Copyright Clearance Center Code: 0741-3106/99/$10.00
Language: English
Abstract: We report the first fabrication of inverted-staggered back-channel-etch hydrogenated amorphous-silicon (a-Si:H) thin-film transistors (TFTs) with a planarized Cu gate electrode. The Cu gate-planarized (GP) a-Si:H TFTs, incorporating benzocyclobutene and a-**SiN**/sub x/:H as a double-layer gate **insulator** , had a field-effect mobility of 0.75 cm/sup 2//V-s, a threshold voltage of 4.92 V, and a subthreshold swing (S) of 0.48 V/dec. These results demonstrate that the GP-TFTs can have an electrical performance comparable with the conventional TFTs without gate planarization. Thus, the gate planarization technology is suitable for application in large-area and high-resolution active-**matrix liquid-crystal** displays.
Subfile: B

35/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6098100 INSPEC Abstract Number: B9901-2560R-053
Title: Stability of the gate **dielectric** /a-Si:H interface with hydrogen plasma treatment
Author(s): Lu, I.-M.; Chen, Y.-E.; Huang, T.-H.; Lin, H.-C.
Author Affiliation: Electron. Res. & Service Org., Ind. Technol. Res. Inst., Hsinchu, Taiwan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3421 p.163-7
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1998 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1998)3421L.163:SGDI;1-N
Material Identity Number: C574-98169
U.S. Copyright Clearance Center Code: 0277-786X/98/$10.00
Conference Title: Display Technologies II
Conference Sponsor: SPIE

Conference Date: 9-11 July 1998 Conference Location: Taipei, Taiwan
Language: English
Abstract: Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) with single-layer gate **insulator** have been stressed with DC bias to investigate the device performance. A low defect density interface between the gate **insulator** (SiNx) and the a-Si:H film is one of the most important factors to obtain high device performance. For the back-channel-etched (BCE) type TFTs, gate SiNx is deposited before the a-Si:H film, and the hydrogen plasma was used to treat the SiNx **insulator** surfaces. From the results of stress experiments, exposing SiNx to hydrogen plasma leads to the charge trapping in the SiNx **insulator** and the state creation in the a-Si:H film. Consequently, the hydrogen plasma treatment of the SiNx surface affects not only the SiNx **insulator** but also the post-deposited a-Si:H film.
Subfile: B

35/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5926154 INSPEC Abstract Number: B9807-2560R-012
Title: Reliability improvements for an a-Si TFT **matrix** by using Al:Ti alloy
Author(s): Zhao, Y.; Xiong, S.; Gu, C.; Wang, Z.P.; Zhou, Z.; Meng, Z.; Li, J.; Dai, Y.; Yao, L.; Zhang, J.J.; Ding, S.; Sun, Z.L.; Geng, W.D.; Li, H.Y.; Li, D.L.
Author Affiliation: Nankai Univ., Tianjin, China
Conference Title: 1996 SID International Symposium. Digest of Technical Papers. First Edition p.345-8
Publisher: Soc. Inf. Display, Santa Ana, CA, USA
Publication Date: 1996 Country of Publication: USA xx+1022 pp.
Material Identity Number: XX96-00687
Conference Title: Proceedings of SID '96
Conference Date: 12-17 May 1996 Conference Location: San Diego, CA, USA
Language: English
Abstract: By using Al:Ti alloy as the gate and source lines and Al/sub 2/O/sub 3//**SiN**/sub x/ as gate **insulator**, the reliability of the a-Si TFT **matrix** was improved. The stability of a-Si TFT with Al/sub 2/O/sub 3//**SiN**/sub x/ double gate **insulator** is much better than that with single **SiN**/sub x/ **insulator**.
Subfile: B

35/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

5888573 INSPEC Abstract Number: B9805-7260-076
Title: Benzocyclobutene **dielectric** resins for flat panel display applications
Author(s): Radler, M.J.; Perettie, D.J.; Den Boer, W.; Gu, T.; Friends, M.
Author Affiliation: Dow Chem. Co., Midland, MI, USA
Conference Title: 1996 Display Manufacturing Technology Conference. Digest of Technical Papers. First Edition p.123-4
Publisher: Soc. Inf. Dsipaly, Santa Ana, CA, USA
Publication Date: 1996 Country of Publication: USA iv+149 pp.

Material Identity Number: XX96-00112
Conference Title: Proceedings of 3rd Annual Display Manufacturing Technology Conference
Conference Date: 6-8 Feb. 1996 Conference Location: San Jose, CA, USA
Language: English
Abstract: Cyclotene/sup TM/ Advanced Electronics Resins offer new opportunities for product differentiation in the highly competitive AMLCD marketplace. In this paper we demonstrate their use as passivation materials for thin film transistors. Back channel etched amorphous silicon transistors passivated with benzocyclobutene (BCB) films show low leakage current and acceptable "on" current. With a **dielectric** constant less than half that of **silicon nitride**, BCB will lower capacitive coupling and signal delay. The transistor structures and surrounding topography are also fully planarized. The planarized active **matrix** should improve contrast and reduce disclinations in the **liquid crystal**. With demonstrated performance as TFT passivation, the low **dielectric** constant and high planarization of Cyclotene/sup TM/ resins may enable unique new TFT structures.
Subfile: B

35/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

5780730 INSPEC Abstract Number: B9801-2560R-077
Title: Self-passivated copper gates for thin film silicon transistors
Author(s): Sirringhaus, H.; Theiss, S.D.; Kahn, A.; Wagner, S.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Conference Title: Amorphous and Crystalline Insulating Thin Films - 199. Symposium p.59-64
Editor(s): Warren, W.L.; Devine, R.A.B; Matsumura, M.; Cristoloveanu, S.; Homma, Y.; Kanicki, J.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1997 Country of Publication: USA xii+440 pp.
Material Identity Number: XX97-01862
Conference Title: Amorphous and Crystalline Insulating Thin Films - 1996. Symposium
Conference Date: 2-4 Dec. 1996 Conference Location: Boston, MA, USA
Language: English
Abstract: A solution to the thin film silicon transistor gate metallization problem in active **matrix liquid crystal** displays is demonstrated in the form of a self-passivation process for copper. Bottom-level copper (Cu) lines are passivated by a self-aligned CrO/sub x/ encapsulation formed by surface segregation of chromium (Cr) from dilute Cu/sub 1-x/Cr/sub x/ alloys (x=0.1-0.3) at 400 degrees C. The encapsulation is an efficient barrier for Cu diffusion into the **SiN** /sub x/ gate **insulator** during the plasma deposition and transistor processing, and solves the problems of oxidation and adhesion to the glass substrate. Gate line resistivities are 4.5 to 7.5 mu Omega cm depending on the initial Cr concentration. The performance of self-passivated Cu-gate thin film transistors is comparable to that of transistors with refractory metal gates.
Subfile: B

35/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

5737850 INSPEC Abstract Number: B9712-7260-024
Title: A two-diode pixel circuit and addressing method for MIM LCDs
Author(s): den Boer, W.
Author Affiliation: OIS Opt. Imaging Syst. Inc., Northville, MI, USA
Conference Title: Proceedings of the Sixteenth International Display Research Conference. SID's 16th International Display Research Conference. EURO DISPLAY p.25-8
Publisher: Soc. Inf. Display (SID), New York, NY, USA
Publication Date: 1996 Country of Publication: USA xvii+633 pp.
Material Identity Number: XX96-03056
Conference Title: Proceedings of 16th International Display Research Conference
Conference Date: 1-3 Oct. 1996 Conference Location: Birmingham, UK
Language: English
Abstract: A pixel circuit with two metal-**insulator**-metal diodes per pixel for AMLCDs is presented, in which each diode is connected to separate select lines. SPICE simulations indicate that this circuit has, compared to conventional MIM pixel circuits, faster response time, increased tolerance for RC delays on the row lines and greatly improved spatial and temporal gray shade uniformity.
Subfile: B

35/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

5727285 INSPEC Abstract Number: A9723-8115H-007, B9712-0520F-007
Title: Substrate effect on plasma-enhanced chemical vapor deposited **silicon nitride**
Author(s): Sherman, S.; Wagner, S.; Mucha, J.; Gottscho, R.A.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Journal: Journal of the Electrochemical Society vol.144, no.9 p. 3198-204
Publisher: Electrochem. Soc,
Publication Date: Sept. 1997 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199709)144:9L.3198:SEPE;1-0
Material Identity Number: J010-97010
U.S. Copyright Clearance Center Code: 0013-4651/97/$7.00
Language: English
Abstract: **Silicon nitride** (**SiN**) deposited by plasma-enhanced chemical vapor deposition (PECVD) is the **dielectric** of choice for use in amorphous silicon thin-film transistors for active-**matrix liquid crystal** displays. Our nitride films deposited in a 40 MHz, coldwall PECVD system on chromium-coated glass substrates exhibit lower etch rates in buffered HF, as well as lower hydrogen contents, lower deposition rates, and higher indexes of refraction than nitride films deposited under supposedly identical conditions on bare glass. We use a simple heat-flow model to show that thermal radiation from the substrate surface in the heated susceptor/coldwall design of our deposition chamber leads to different substrate temperatures for different surface types, thus causing the substrate dependent deposition. We present **SiN** film data as a function of temperature and as a function of thickness to support this theory. Additionally, the length scale over which this thermal effect is relevant, and its effect on film and device uniformity, are discussed.
Subfile: A B

35/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

5718388 INSPEC Abstract Number: B9711-7260-088
Title: Self-passivated copper gates for amorphous silicon thin film transistors
Author(s): Sirringhaus, H.; Kahn, A.; Wagner, S.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3014 p.62-9
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1997 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1997)3014L.62:SPCG;1-1
Material Identity Number: C574-97131
U.S. Copyright Clearance Center Code: 0277-786X/97/$10.00
Conference Title: Active Matrix Liquid Crystal Displays Technology and Applications
Conference Sponsor: SPIE; Soc. Imaging Sci. & Technol
Conference Date: 10-11 Feb. 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: A solution to the thin film silicon transistor gate metallization problem in active **matrix liquid crystal** displays is demonstrated in the form of a self-passivation process for copper. Bottom-level copper (Cu) lines are passivated by a self-aligned chromium oxide encapsulation formed by surface segregation of chromium (Cr) from dilute Cu/sub 1-x/Cr/sub x/ alloys at 400 degrees C. The encapsulation is an efficient barrier for Cu diffusion into the **SiN**/sub x/ gate **insulator** during the plasma deposition and transistor processing, and solves the problems of oxidation and adhesion to the glass substrate without introducing additional mask steps into the manufacturing process. Gate line resistivities of 4.5 mu Omega .cm are obtained. The performance of self-passivated Cu-gate thin film transistors is comparable to that of transistors with refractory metal gates.
Subfile: B

35/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

5622420 INSPEC Abstract Number: B9708-7260-047
Title: The substrate's effect on PECVD **silicon nitride**
Author(s): Sherman, S.; Wagner, S.; Mucha, J.; Gottscho, R.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Conference Title: Proceedings of the Third Symposium on Thin Film Transistor Technologies p.328-41
Editor(s): Kuo, Y.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA xil+404 pp.
Material Identity Number: XX96-02895
Conference Title: Proceedings of Thin Film Transistor Technologies III (ISBN 1 56677 173 0)
Conference Sponsor: Electrochem. Soc
Conference Date: 7-11 Oct. 1996 Conference Location: San Antonio, TX,

USA
Language: English
Abstract: **Silicon nitride** (**SiN**) deposited by plasma-enhanced chemical vapor deposition (PECVD) is the **dielectric** of choice for use in amorphous silicon thin-film transistors (TFTs) for active-**matrix liquid crystal** displays. Nitride films deposited in a 40 MHz, cold-wall PECVD system on chromium-coated glass substrates exhibit lower etch rates in buffered HF acid, as well as lower hydrogen contents, lower deposition rates, and higher refractive indices than nitride films deposited under supposedly identical conditions on bare glass. We use a simple heat-flow model to show that thermal radiation from the substrate surface in the heated-susceptor/cold-wall design of our deposition chamber leads to different substrate temperatures for different surface types, thus causing substrate-dependent deposition.
Subfile: B

35/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

5423954 INSPEC Abstract Number: A9624-8115C-013, B9612-0520F-087
Title: Large area deposition: sputtering- and PCVD-systems and techniques for **LCD**
Author(s): Hosokawa, N.
Author Affiliation: R&D Div., Anelva Corp., Tokyo, Japan
Journal: Thin Solid Films Conference Title: Thin Solid Films (Switzerland) vol.281-282, no.1-2 p.136-42
Publisher: Elsevier,
Publication Date: 1 Aug. 1996 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19960801)281/282:1/2L.136:LADS;1-R
Material Identity Number: T070-96017
U.S. Copyright Clearance Center Code: 0040-6090/96/$15.00
Conference Title: 13th International Vacuum Congress and 9th International Conference on Solid Surfaces
Conference Date: 25-29 Sept. 1995 Conference Location: Yokohama, Japan
Language: English
Abstract: In the fabrication of **liquid crystal** displays (LCDs) having a thin film transistor active **matrix**, as used in personal computers, several films are deposited by plasma enhanced chemical vapour deposition (PCVD) and sputtering methods. Semiconducting a-Si:H films and **insulating** a-**SiN** films are synthesized from SiH/sub 4/, H/sub 2/, NH/sub 3/, and N/sub 2/ gases in PCVD systems using parallel plate RF electrodes. Interconnect and electrode films of Cr, Ti, Mo, Ta, Al, and indium-tin oxide are deposited in sputtering systems having planar magnetron cathodes. Large area glass substrates, ranging from 300 mm*400 mm to 400 mm*500 mm, are processed. Typical systems are categorized as in-line tray transfer or single substrate transfer cluster tool types. The configurations, key components, deposition processes, and film properties are described.
Subfile: A B

35/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

4805235 INSPEC Abstract Number: B9412-7260-022

03/25/2003

Title: An **LCD** addressed by a-Si:H TFTs with peripheral poly-Si TFT circuits
Author(s): Tanaka, T.; Asuma, H.; Ogawa, K.; Shinagawa, Y.; Ono, K.; Konishi, N.
Author Affiliation: Res. Lab., Hitachi Ltd., Ibaraki, Japan
p.389-92
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA 940 pp.
ISBN: 0 7803 1450 6
U.S. Copyright Clearance Center Code: 0 7803 1450 6/93/$3.00
Conference Title: Proceedings of IEEE International Electron Devices Meeting
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 5-8 Dec. 1993 Conference Location: Washington, DC, USA
Language: English
Abstract: Poly-Si TFTs of an inverted staggered structure are fabricated by peripheral laser annealing of plasma CVD a-Si:H films on **SiN** gate **insulator** . The side contact structure improves the TFT characteristics resulting in mobility of 20 cm/sup 2//Vs and on/off ratio of 10/sup 6/. The fabrication process, carried out below 300 degrees C, is compatible with conventional a-Si TFT processes. The **LCD** using a switch **matrix** of poly Si TFTs has good performance and reduces the number of driver ICs by half.
Subfile: B

35/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

4735598 INSPEC Abstract Number: B9409-2560R-097
Title: Steady state and pulsed bias stress induced degradation in amorphous silicon thin film transistors for active-**matrix** **liquid crystal** displays
Author(s): Libsch, F.R.
Author Affiliation: Res. Div., IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
p.681-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA 1022 pp.
ISBN: 0 7803 0817 4
U.S. Copyright Clearance Center Code: 0 7803 0817 4/92/$3.00
Conference Title: Proceedings of IEEE International Electron Devices Meeting
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 13-16 Dec. 1992 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The threshold voltage instabilities in nitride/oxide dual gate **dielectric** hydrogenated amorphous silicon (a-Si:H) thin-film transistors are investigated as a function of stress time, stress temperature and stress bias. The obtained results are explained with a multiple trapping model, rather than weak bond breaking model. In our model, the injected carriers from the a-Si:H channel first thermalize in a broad distribution of localized band-tail states located at the a-Si:H/a-**SiN**/sub x/:H interface and in the a-**SiN**/sub x/:H transitional layer close to the interface, then move to deeper energies in amorphous **silicon nitride** at longer stress times, larger stress electric fields, or higher stress temperatures. The results of the model are consistent with the bias-stress-temperature data. Steady state (DC) as well

as pulsed bias stress measurements have been employed to electrically characterize the instabilities in a-Si:H TFTs.
Subfile: B

35/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

03192382 INSPEC Abstract Number: B88053777
Title: Driving scheme of **LCD**
Author(s): Yanagisawa, T.
Author Affiliation: Electron Device Eng. Lab., Toshiba Corp., Yokohama, Japan
Journal: Journal of the Institute of Television Engineers of Japan vol.42, no.1 p.10-16
Publication Date: Jan. 1988 Country of Publication: Japan
CODEN: JITJA7 ISSN: 0386-6831
Language: Japanese
Abstract: The structure of a colour **LCD** and its driving scheme using a single **matrix** or active **matrix** are outlined with the time division multiplexing of a signal for single **matrix** using TFT or MIM for an active **matrix**. The TFT-**LCD** a-Si type and poly-Si type are described. Driving parameters for TFT and prevention of flicker are examined. The viewing angle of TFT-**LCD** is +or-35 degrees left-right and +or-30 degrees up-down with a constant ratio of 20:1. Active **matrix** type LCDs using non-linear elements are discussed including metal-**insulator**-metal, pin-diode ring, off stoichiometric **SiN** /sub x/ diode, and back-to-back diode, and their driving systems are briefly discussed.
Subfile: B

35/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

03155778 INSPEC Abstract Number: B88042207
Title: A new active diode **matrix LCD** using off-stoichiometric **SiN**/sub x/ layer
Author(s): Suzuki, M.; Toyama, M.; Harajiri, T.; Maeda, T.; Yamazaki, T.
Author Affiliation: Seiko Instrum. Inc., Matsudo, Japan
Journal: Proceedings of the S.I.D vol.28, no.2 p.101-4
Publication Date: 1987 Country of Publication: USA
CODEN: SIDPAA ISSN: 0734-1768
U.S. Copyright Clearance Center Code: 0734-1768/87/2802-0101$1.00
Conference Title: 6th International Display Research Conference: Japan Display '86
Conference Sponsor: SID; Inst. Telev. Eng. Japan
Conference Date: 30 Sept.-2 Oct. 1986 Conference Location: Tokyo, Japan
Language: English
Abstract: An active-**matrix LCD** utilizing a new type of two-terminal element is described. The two-terminal nonlinear element, consisting of metal/off-stoichiometric **SiN** /sub x//ITO (indium tin oxide), shows symmetric steep diode characteristics and is stable under 40000 hours of continuous operation. The new two-terminal element was applied to the **matrix**-addressed **LCD** to investigate the driving performance. An **LCD** with 128*160 pixels was fabricated and can realize a contrast ratio greater than 8 for a reflection-type panel with a duty ratio lower than 1/1000. Since the two-terminal element composed of

three thin-film layers can be produced by a simple fabrication process, LCDs containing those elements have the advantages of low cost and large area.
Subfile: B

35/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

03079049 INSPEC Abstract Number: B88016323
Title: A large-area diode-**matrix LCD** using **SiN**/sub x/ layer
Author(s): Toyama, M.; Harajiri, T.; Maeda, T.; Kuroda, Y.; Tsunoda, Y.; Suzuki, M.; Yamazaki, T.
Author Affiliation: Seiko Instrum. Inc., Chiba, Japan
Conference Title: 1987 SID International Symposium. Digest of Technical Papers. First Edition p.155-8
Editor(s): Morreale, J.
Publisher: Palisades Inst. Res. Services, New York, NY, USA
Publication Date: May 1987 Country of Publication: USA x+465 pp.
U.S. Copyright Clearance Center Code: 0097-0966X/87/0000-155-$1.00+.00
Conference Date: 12-14 May 1987 Conference Location: New Orleans, LA, USA
Language: English
Abstract: On the basis of the result, the authors have developed a large area (9.8 inch diagonal) diode **matrix LCD** with 640*400 pixels. They have also developed a process which makes use of only two masks. The large area **LCD** shows high contrast ratio and excellent horizontal uniformity of display.
Subfile: B

35/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

02111754 INSPEC Abstract Number: B83051762
Title: Amorphous-silicon FET array for **LCD** panel
Author(s): Katoh, K.; Yasui, M.; Kuniyasu, S.; Watanabe, H.
Author Affiliation: Res. & Dev. Lab., Stanley Electric Co., Yokohama, Japan
Journal: Electronics Letters vol.19, no.14 p.506-7
Publication Date: 7 July 1983 Country of Publication: UK
CODEN: ELLEAK ISSN: 0013-5194
Language: English
Abstract: A small 20*20 dot **matrix** array has been fabricated on a glass substrate using a-Si films as the semiconductor and **silicon nitride** deposited from a N/sub 2/-SiH/sub 4/ mixture as the gate **insulator**. Good operation is obtained for both TN-mode and GH-mode in transparent-type LCDs. The improved fabrication process and structure are reported.
Subfile: B

35/3,AB/22 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06279471
E.I. No: EIP03047336130

Title: The use of C-V techniques to investigate instability mechanisms in M-I-S structures
Author: Shashi, Paul; Milne, W.I.; Robertson, J.
Corporate Source: Ctr. for Molec. Nanoscale Electron. School of Engineering University of Durham, Durham DH1 3LE, United Kingdom
Conference Title: Silicon Materials - Processing, Characterization and Reliability
Conference Location: San Francisco, CA, United States Conference Date: 20020401-20020405
E.I. Conference No.: 60609
Source: Materials Research Society Symposium - Proceedings v 716 2002. p 477-482
Publication Year: 2002
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Abstract: In the field of flat panel displays, the current leading technology is the Active **Matrix liquid Crystal** Display; this uses a-Si:H based thin film transistors (TFTs) as the switching element in each pixel. However, under gate bias a-Si:H TFTs suffer from instability, as is evidenced by a shift in the gate threshold voltage. The shift in the gate threshold voltage is generally measured from the gate transfer characteristics, after subjecting the TFT to prolonged gate bias. However, a major drawback of this measurement method is that it cannot distinguish whether the shift is caused by the change in the midgap states in the a-Si:H channel or by charge trapping in the gate **insulator**. In view of this, we have developed a capacitance-voltage (C-V) method to measure the shift in threshold voltage. We employ Metal-**Insulator** -Semiconductor (MIS) structures to investigate the threshold voltage shift as they are simpler to fabricate than TFTs. We have investigated a large of number Metal/a-Si:H/Si//3N//4/**Si*****n** structures using our C-V technique. From, the C-V data for the MIS structures, we have found that the relationship between the thermal energy and threshold voltage shift is similar to that reported by Wehrspohn et. al in a-Si:H TFTs (J Appl. Phys, 144, 87, 2000). The a-Si:H and Si//3N//4 layers were grown using the radio-frequency plasma-enhanced chemical vapour deposition technique. 7 Refs.

35/3,AB/23 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05264895
E.I. No: EIP99034612124
Title: Planarized copper gate hydrogenated amorphous-silicon thin-film transistors for AM-**LCD**'s
Author: Lan, Je-Hsiung; Kanicki, Jerzy
Corporate Source: Univ of Michigan, Ann Arbor, MI, USA
Source: IEEE Electron Device Letters v 20 n 3 Mar 1999. p 129-131
Publication Year: 1999
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: We report the first fabrication of inverted-staggered back-channel-etch hydrogenated amorphous-silicon (a-Si:H) thin-film transistors (TFT's) with a planarized Cu gate electrode. The Cu gate-planarized (GP) a-Si:H TFT's, incorporating benzocyclobutene and a-**SiN**//x: H as a double-layer gate **insulator**, had a field-effect mobility of 0.75 cm**2/V-s, a threshold voltage of 4.92 V, and a subthreshold swing (S) of 0.48 V/dec. These results demonstrate that the GP-TFT's can have an electrical performance comparable with the conventional TFT's without gate planarization. Thus, the gate planarization

technology is suitable for application in large-area and high-resolution active-**matrix liquid-crystal** displays. (Author abstract)
9 Refs.

35/3,AB/24 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10558194 Genuine Article#: 541PR Number of References: 35
Title: Hot wire deposited materials for thin film transistors (ABSTRACT AVAILABLE)
Author(s): Schropp REI; Stannowski B; Rath JK
Corporate Source: Univ Utrecht,Debye Inst,NL-3508 TA Utrecht//Netherlands/
Journal: INFORMACIJE MIDEM-JOURNAL OF MICROELECTRONICS ELECTRONIC COMPONENTS AND MATERIALS, 2001, V31, N4 (DEC), P220-227
ISSN: 0352-9045 Publication date: 20011200
Publisher: SOC MICROELECTRONICS, ELECTRON COMPONENTS MATERIALS-MIDEM, DUNAJSKA 10, LJUBLJJANA 61000, SLOVENIA
Language: English Document Type: ARTICLE
Abstract: Thin film transistors (TFTs) find widespread application as the switching element in active **matrix** (AM) **liquid crystal** displays (**LCD**), such as the TFT display used in lap top computers, but also in 2-dimensional imaging devices, such as document scanners or in digital X-ray imagers for medical applications.

This paper addresses the new challenges that exist in research and development of TFTs: 1) TFT's on plastic substrates, 2) low-temperature poly-silicon (LTPS) for the pixel TFTs and for row and column drivers on glass; 3) addressing of OLEDs (Organic Light Emitting Diodes) by silicon TFTs. For these advanced applications of TFTs the relevant issues are: (i) higher electron mobility, (ii) stability, and (iii) defect free, uniform deposition of thin silicon films and gate dielectrics at a high deposition rate (for reduced cost). Whereas a high deposition rate is generally needed to reduce the production cost, for novel high current applications the latter two issues have recently become more essential.

At Utrecht University, we are investigating Hot Wire (Catalytic) CVD as a deposition technique for novel TFTs that have a high potential to meet the above mentioned requirements, In Hot Wire CVD, the source gases are catalytically decomposed at heated tungsten or tantalum filaments (similar to1800 degreesC), whereas the substrate is kept at a low temperature. Hydrogenated amorphous silicon (a-Si:H) with device quality can be deposited at a high rate of 1-5 nm/s. Bottom gate, inverted staggered TFTs with Hot Wire CVD silicon films have been made with an electron mobility of 1.5 cm(2)/VS, and with field effect characteristics that are completely stable under operating conditions. Top gate, coplanar TFTs with polycrystalline silicon films have been made, showing a mobility of 4.7 cm(2)/Vs, in agreement with the Hall mobility measured in individual thin films, This has been obtained without any post deposition treatment, and the Hot Wire technology can thus avoid expensive, time-consuming steps such as the laser recrystallization step that is currently used in the production of the latest poly-Si lap top displays, Hot Wire CVD is also suitable for the deposition of **silicon nitride** (SiNx:H) gate dielectrics.
TFTs with a Hot Wire **silicon nitride** gate **dielectric**, deposited below 400 degreesC, have reached a mobility of 0.6 cm(2)/Vs and a threshold voltage of 2.9 V.

03/25/2003

35/3,AB/25 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08714818 Genuine Article#: 320GL Number of References: 10
Title: Amorphous silicon thin-film transistor with fluorinated silicon oxide ion stopper (ABSTRACT AVAILABLE)
Author(s): Kim KW (REPRINT) ; Cho KS; Ryu JI; Yoo KH; Jang J
Corporate Source: KYUNG HEE UNIV,DEPT PHYS/SEOUL 130701//SOUTH KOREA/ (REPRINT)
Journal: IEEE ELECTRON DEVICE LETTERS, 2000, V21, N6 (JUN), P301-303
ISSN: 0741-3106 Publication date: 20000600
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: We propose fluorinated silicon oxide (SiOF) as the ion-stopper of bottom-gate amorphous silicon thin film transistors (a-Si:H TFT's). The low **dielectric** constant SiOF on both back-channel of the TFT and the crossover regions of gate/data lines can contribute to reducing the RC delay of the gate pulse signal in active-**matrix liquid-crystal** displays. Besides, an a-Si:H TFT with a SiOF stopper had an improved performance compared to a widely-employed **silicon nitride** (SiNx) stopper TFT because the fluorine incorporation reduces the interface state density between a-Si:H and SiOF.

35/3,AB/26 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05954381 Genuine Article#: XJ925 Number of References: 32
Title: Nanoscale patterning of barium titanate on block copolymers (ABSTRACT AVAILABLE)
Author(s): Lee T; Yao N; Aksay IA (REPRINT)
Corporate Source: PRINCETON UNIV,DEPT CHEM ENGN/PRINCETON//NJ/08544 (REPRINT); PRINCETON UNIV,DEPT CHEM ENGN/PRINCETON//NJ/08544; PRINCETON UNIV,PRINCETON MAT INST/PRINCETON//NJ/08544
Journal: LANGMUIR, 1997, V13, N14 (JUL 9), P3866-3870
ISSN: 0743-7463 Publication date: 19970709
Publisher: AMER CHEMICAL SOC, 1155 16TH ST, NW, WASHINGTON, DC 20036
Language: English Document Type: ARTICLE
Abstract: A triblock copolymer of polystyrene-polybutadiene-polystyrene (Kraton D1102) has been used to pattern barium titanate precursor with nanoscale modulations. The copolymer self-assembles to yield cylindrical polystyrene nanodomains in a polybutadiene **matrix**. The preorganized thin films of polymer are then selectively OH-functionalized in situ on the unsaturated carbon bonds in the polybutadiene **matrix** with antistereochemistry. Anchoring the barium titanate precursor onto the hydroxylated polymer thin films is possible only in the trans-1,2 polybutadiol **matrix** through the condensation between the barium titanium double alkoxides and the hydroxyl groups. The regioselective deposition of the barium titanium double alkoxides on the original polybutadiene **matrix** of the Kraton thin films was verified by transmission electron microscopy and electron energy loss spectroscopy. The spacing of the coordinated barium titanium double alkoxide pattern was similar to 23 nm, equivalent to the interdomain spacing of the original polybutadiene **matrix**.

35/3,AB/27 (Item 4 from file: 34)

03/25/2003

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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05204564 Genuine Article#: VH138 Number of References: 8
Title: LARGE-AREA DEPOSITION - SPUTTERING-SYSTEMS AND PCVD-SYSTEMS AND TECHNIQUES FOR **LCD** (Abstract Available)
Author(s): HOSOKAWA N
Corporate Source: ANELVA CORP,R&D DIV,8-1,5 CHOME/FUCHU/TOKYO 183/JAPAN/
Journal: THIN SOLID FILMS, 1996, V282, N1-2 (AUG 1), P136-142
ISSN: 0040-6090
Language: ENGLISH Document Type: ARTICLE
Abstract: In the fabrication of **liquid crystal** displays (LCDs) having a thin film transistor active **matrix**, as used in personal computers, several films are deposited by plasma enhanced chemical vapour deposition (PCVD) and sputtering methods. Semiconducting a-Si:H films and **insulating** a-**SiN** films are synthesized from SiH4, H2, NH3, and N2 gases in PCVD systems using parallel plate RF electrodes, Interconnect and electrode films of Cr, Ti, Mo, Ta, Al, and indiumu-tin oxide are deposited in sputtering systems having planar magnetron cathodes. Large area glass substrates, ranging from 300 mm X 400 mm to 400 mm X 500 mm, are processed. Typical systems are categorized as in-line tray transfer or single substrate transfer cluster tool types. The configurations, key components, deposition processes, and film properties are described.

35/3,AB/28 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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03860232 Genuine Article#: QM604 Number of References: 69
Title: ON A MAPPING BETWEEN HARD-CORE POTENTIAL MODELS FOR NEMATOGENS AND CONTINUOUS ONES (Abstract Available)
Author(s): ROMANO S
Corporate Source: UNIV PAVIA,DIPARTIMENTO FIS A VOLTA,VIA A BASSI6/I-27100 PAVIA//ITALY/
Journal: INTERNATIONAL JOURNAL OF MODERN PHYSICS B, 1995, V9, N1 (JAN 10) , P85-102
ISSN: 0217-9792
Language: ENGLISH Document Type: ARTICLE
Abstract: Hard-core nematogenic models can be studied using Onsager's theory, and, on the other hand, continuous interaction potentials can be investigated using the molecular field approach pioneered by Maier and Saupe. Comparison between these treatments shows a certain formal similarity, reflecting their common variational root; on this basis, hardcore potential models can be mapped on separable continuous ones, via their excluded volume. As a specific example, we have, therefore, considered hard spherocylinders and hence the continuous potential model(s)

[GRAPHICS]

here u(j) denotes the unit vector defining particle orientation, x(j) denotes the coordinate vector of its center of mass, and epsilon is a positive quantity setting temperature and energy scales(i.e. T-* = k(B)T/epsilon). The **sin**\ function can be expanded in a series of Legendre polynomials of even order, with a dominant P-2 term; particles' centers of mass were associated with a simple-cubic lattice, the function phi(r) was truncated at nearest-neighbor separation, and values of the two parameters p and q were chosen so as to make contact with the Lebwohl-Lasher lattice model, i.e. phi(1) = 1, p = -8/5, q = 32/5 pi. The resulting pair potential was studied by molecular field

theory and by computer simulation; molecular field theory predicts a first-order transition at T-c*,(MF) = 1.356, whereas the result obtained by simulation was T-c* = 1.235 +/- 0.005; comparison with the Lebwohl-Lasher model shows that the higher-order interactions contained in the potential tend to increase the transition temperature towards its molecular field limit.

35/3,AB/29 (Item 6 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01824449 Genuine Article#: JD825 Number of References: 7
Title: STUDY OF THE 5TH SHIFT OF THE THIN-FILM TRANSISTOR BY THE BIAS TEMPERATURE STRESS TEST (Abstract Available)
Author(s): FUJIMOTO Y
Corporate Source: IBM JAPAN LTD,DISPLAY TECHNOL,1623-14 SHIMOTSURUMA/YAMATO/KANAGAWA 242/JAPAN/
Journal: IBM JOURNAL OF RESEARCH AND DEVELOPMENT, 1992, V36, N1 (JAN), P 76-82
Language: ENGLISH Document Type: ARTICLE
Abstract: Amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as the switching device in the active-**matrix** addressing of **liquid crystal** displays. One concern is the potential instability problems associated with the threshold voltage (V(th)) shifts to higher values after prolonged operating times. The reason for this V(th) shift has been widely discussed, and two models accounting for it have been suggested. One model explains the shifts by the trapping of electrons in the **insulator**, the other model by the creation of the metastable states at the a-Si:H/**SiN**(x) interface. Our TFT **insulator** has the rather complicated structure of an anodic oxide film, SiO(x), **SiN**(x) sequentially stacked over the gate electrode, which makes it difficult to separate the contribution of each layer. To confirm the V(th) shift mechanism and the contribution of each layer of **insulator** to the V(th) shift, we have prepared samples with a series of different **insulators** and have measured the blas dependence of their V(th) shifts. Our results show that the anodic oxide film makes no contribution to the V(th) shift, and it makes little difference to the V(th) shift whether the next **insulator** is **SiN**(x) or SiO(x). The latter fact may be explained in two ways. One is that both **SiN**(x) and SiO(x) make the same contribution to the V(th) shift. Alternatively, neither **SiN**(x) nor SiO(x) makes any contribution to the V(th) shift, but the a-Si:H/gate **insulator** interface has some contribution. From these experiments, it cannot be determined which of the proposed mechanisms is consistent with the behavior of the V(th) shift of our a-Si:H TFT.

35/3,AB/30 (Item 7 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01519857 Genuine Article#: HE981 Number of References: 12
Title: PLASMA ENHANCED CVD FOR FLAT PANEL DISPLAYS (Abstract Available)
Author(s): CROWLEY JL
Corporate Source: OMARA & ASSOCIATES/PALO ALTO//CA/00000
Journal: SOLID STATE TECHNOLOGY, 1992, V35, N2 (FEB), P94&
Language: ENGLISH Document Type: ARTICLE
Abstract: Plasma enhanced chemical vapor deposition (PECVD) is the preferred deposition method for many thin films used in active

matrix liquid crystal flat panel displays (AMLCD). It is especially suited for depositing the hydrogenated amorphous silicon (alpha-Si:H) active semiconductor layer and is also used to deposit gate and field **dielectric** thin films such as SiNx and SiO2. This article reviews PECVD with respect to film properties, processes, and equipment for flat panel displays.

35/3,AB/31 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01778674 AADAAI9990947
Amorphous silicon thin-film transistor active-**matrix** for reflective cholesteric **liquid crystal** displays
Author: Nahm, Jeong-Yeop
Degree: Ph.D.
Year: 2000
Corporate Source/Institution: University of Michigan (0127)
Source: VOLUME 61/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5480. 108 PAGES
ISBN: 0-599-98487-2

Reflective cholesteric **liquid crystal** displays (Ch-LCDs) have advantages, such as, high brightness, low power consumption, and wide viewing angle, since they do not need any polarizer, color filter, and backlight. Furthermore, due to their bistability Ch-LCDs can retain their images virtually forever without additional power consumption. But conventional passive-**matrix** addressing of Ch-LCDs allows only a slow image updating speed. Active-**matrix** addressing should allow fast image updating or video-rate operation. However, because the threshold voltage of cholesteric, **liquid crystal** is high (>20V), the switching devices for active-**matrix** addressing should satisfy required characteristics even under high bias conditions. In order to investigate the applicability of hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) for the switching devices of active-**matrix** (AM) Ch-LCDs, the characteristics of conventional and gate offset high voltage a-Si:H TTFs were examined under high bias conditions. And it was concluded that high OFF-current of conventional a-Si:H TFTs and low ON-current of gate offset high voltage a-Si:H TFTs were main problems for reflective AM Ch-**LCD** applications. In order to improve the TFT characteristics under high bias conditions, we propose two new a-Si:H TFT structures called gate planarized (GP) and buried field plate (BFP) high voltage a-Si:H TFTs. Firstly, in the GP a-Si:H TFTs, we used a thick spin-coated benzocyclobutene (BCB) layer beneath a thin hydrogenated amorphous **silicon nitride** (a-**SiN**_x:H) layer for gate **insulator**. The GP a-Si:H TFT showed normal TFT characteristic up to V_{GS} = V_{DS} = ∼100 V without any device failure. But TFT ON-current of GP a-Si:H TFT was reduced due to the introduction of the thick low **dielectric** BCB layer. Secondly, in the BFP a-Si:H TFT, an offset region and a buried field plate were introduced between the drain/source and gate electrodes to reduce the electric field in the pinch-off region. For this BFP a-Si:H TFT, a low OFF-current (1.04 pA) and a high ON/OFF-current ratio (5.68 × 10⁶) up to V_{GS} = V_{DS} = ∼30 V were obtained. Based on our a-Si:H TFTs studies, we designed an a-Si:H TFT active-**matrix** panel and fabricated the AM Ch-LCDs either by optimizing a-Si:H TFT processing or adopting the GP a-Si:H TFT technology. The fabricated a-Si:H TFT active-**matrix** panels can be operated at the voltage of 50 and 60V, applied to the data and gate lines, respectively. With the a-Si:H TFT active-**matrix** panels, the AM Ch-LCDs were fabricated and operated with the

frame rate of 60 Hz and the maximum contrast ratio of ∼30.

35/3,AB/32 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01562561 AAD9718101
PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION ISSUES FOR AMORPHOUS SILICON THIN-FILM TRANSISTORS FOR ACTIVE-**MATRIX LIQUID CRYSTAL** DISPLAYS (CVD, **LCD**, TFT, BAND TAILS)
Author: SHERMAN, STEVEN ROBERT
Degree: PH.D.
Year: 1997
Corporate Source/Institution: PRINCETON UNIVERSITY (0181)
Source: VOLUME 58/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 351. 145 PAGES

A fabrication process for high-quality amorphous silicon (a-Si) thin-film transistors (TFTs) suitable for active-**matrix liquid crystal** display (AMLCD) application has been developed. Two issues concerning the plasma-enhanced chemical vapor deposition (PECVD) unit process have been addressed: the trade-off between the deposition rate of a TFT's a-Si layer and the effective electron mobility of that TFT, and the substrate's effect on the **silicon nitride** (**SiN**) gate **insulator**.

a-Si deposition power, and therefore deposition rate, were identified as important parameters in TFT fabrication by comparing isolated a-Si films deposited at different deposition powers to TFTs with a-Si layers deposited identically to the isolated films. The characteristic energy of the exponential valence-band-tail of the a-Si films, as measured by sub-gap optical-absorption spectroscopy, was found to increase with increasing deposition rate. Also, the effective electron mobility of the TFTs decreases linearly with the valence-band-tail energy. However, subsequent modeling of our TFTs confirmed that the effective mobility is largely controlled by the conduction-band-tail because these are n-channel devices. So faster a-Si deposition was found to cause more localized states near both band edges, thus lowering the effective electron mobility in the TFT. This constitutes the first experimental evidence for a correlation between the characteristic energies of the conduction- and valence-band-tail energies of a-Si.

Silicon nitride film properties, including etch and deposition rate, index of refraction and hydrogen content, were found to depend on the underlying substrate type, for example metal- coated glass versus bare glass. This unexpected phenomenon is attributed to the heated-susceptor/cold-wall design of the deposition chamber. A very simple heat-flow model of the chamber shows that thermal radiation from the substrate surface is a significant heat-loss mechanism. This leads to different substrate temperatures for different substrate types, thus causing the substrate- dependent deposition. Additionally, this effect was found to cause macroscopic film non-uniformities on substrates with metal patterns, such as gate-metal patterns on standard AMLCD TFT arrays.

35/3,AB/33 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01500498 JICST ACCESSION NUMBER: 92A0373219 FILE SEGMENT: JICST-E
Tft technology for large-area flat panel display.
TSUKADA TOSHIHISA (1)

(1) Hitachi, Ltd., Central Res. Lab.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology), 1991, VOL.41st, PAGE.25-30, FIG.4, TBL.1, REF.8
JOURNAL NUMBER: F0108BAP
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: In the late eighties, there has been great progress in TFT/**LCD**(Thin-Flim Transistor activated **Liquid Crystal** Display) technology. The hydrogenated amorphous silicon(a-Si) TFT has become a major device for producing these displays. Most current **LCD** mass-production lines for active-**matrix** displays use this technology. This is because a-Si TFTs are compatible with glass substrates, match the high-resistance **liquid crystal**, and offer good electrical properties. The keywords for the TFT/**LCD** in the nineties are full-color, large diagonal-size, and high resolution. As the display size increases, and as the resolution higher, the gate-line delay problem and the yield of the panel become more important. The double-layered gate **insulator** such as Ta2O5/**SiN** or Al2O3/**SiN**, has therefore been proposed and used in products. The Al-gate TFT reduces gate-line delay and enhance production yield. With this Al-gate TFT, conventional design rules can achieve a diagonal size over 30 inches and resolution over 1 Mpixel(3Mdots). Flat panel displays will play a leading role in the nineties and into the next century. The TFT/**LCD** is the device for creating new display markets other than CRTs. New product concepts as well as new display devices will appear in the next decade to brighten our daily life. (author abst.)

35/3,AB/34 (Item 2 from file: 94)

01205853 JICST ACCESSION NUMBER: 90A0897634 FILE SEGMENT: JICST-E
Special issue on thin film trnasistor technology on glass substrates. II. Amorphous silicon thin film transistors prepared by plasma enhanced chemical vapor deposition.
FUKUDA KAICHI (1); IBARAKI NOBUKI (1)
(1) Toshiba Corp., Electron Device Engineering Lab.
Denki Gakkai Ronbunshi. A(Transactions of the Institute of Electrical Engineers of Japan. A), 1990, VOL.110,NO.10, PAGE.659-666, FIG.16, REF.18
JOURNAL NUMBER: S0808AAA ISSN NO: 0385-4205
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: On amorphous silicon (a-Si) thin film transistor (TFT), this paper describes the following paragraphs.1) the structure.2) manufacturing method and equipment by plasma CVD.3) a-si : **silicon nitride** film to use as H and gate **insulator** material a-Si.4) the effect on properties and TFT characteristics of oxide film.5) the application to **LCD**.A-Si TFT **LCD** was marketed as a **liquid crystal** television, with a 2-5 inche, diagonal and a 10 inch display was also partially commercialized.

37/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7167191 INSPEC Abstract Number: B2002-03-2560R-012
Title: Polymeric organic-inorganic composite gate **insulating** materials for TFTs
Author(s): Kim, G.; Min, K.; Kim, H.; Hwang, Y.; Kim, K.
Author Affiliation: Adv. Mater. Res. Inst., Taejon, South Korea
Conference Title: IDW '00. Proceedings of the Seventh International Display Workshops p.275-8
Publisher: Inst. Image Inf. & Telev. Eng. & Soc. Inf. Display (SID), Tokyo, Japan & San Jose, CA, USA
Publication Date: 2000 Country of Publication: USA xxi+1226 pp.
Material Identity Number: XX-2000-03025
Conference Title: Proceedings of 7th International Display Workshops - IDW'00
Conference Sponsor: Inst. Image Inf. & Telev. Eng.; SID
Conference Date: 29 Nov.-1 Dec. 2000 Conference Location: Kobe, Japan
Language: English
Abstract: Organic/inorganic composite materials have been prepared incorporating metal oxide or metal alkoxide such as **SiO**/sub 2/, TiO/sub 2/ and tetraethoxysilane (TEOS) as the inorganic components with alicyclic polyimides to obtain high **dielectric** constant gate **insulating** materials for a-Si:H TFT. The metal oxide particles were dispersed homogeneously in the **matrix** polyimides as observed by SEM. The hybrid films also exhibit much higher **dielectric** constants epsilon ' (7.8 at 60 wt% TiO/sub 2/) as compared with epsilon '=3.4 for the pure polyimide films.
Subfile: B

37/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7059151 INSPEC Abstract Number: B2001-11-2230-004
Title: The fabrication and electrical characteristics of pentacene TFT using polyimide and polyacryl as a gate **dielectric** layer
Author(s): Yun-Myoung Kim; Ok-Byoung Kim; Young-Kwan Kim; Jung-Soo Kim
Journal: Transactions of the Korean Institute of Electrical Engineers, C vol.50, no.4 p.161-8
Publisher: Korean Inst. Electr. Eng,
Publication Date: April 2001 Country of Publication: South Korea
CODEN: CHNODD ISSN: 1229-246X
SICI: 1229-246X(200104)50:4L.161:FECP;1-K
Material Identity Number: H331-2001-008
Language: Korean
Abstract: Organic thin film transistors (TFTs) are of interest for use in broad area electronic applications. For example, in active **matrix liquid crystal** displays (AMLCDs), organic TFTs would allow the use of inexpensive, light-weight, flexible, and mechanically rugged plastic substrates as an alternative to the glass substrates needed for commonly used hydrogenated amorphous silicon (a-Si:H). Pentacene TFTs with carrier field effect mobility as large as 2 cm/sup 2/ V/sup -1/ s/sup -1/ have been reported for TFTs fabricated on silicon substrates, and it is higher than that of a-Si:H. But these TFTs are fabricated on silicon wafer and **SiO**/sub 2/ was used as a gate **insulator**. **SiO**/sub 2/ deposition process requires a high temperature. We have fabricated organic

pentacene TFTs at lower temperature by using organic material as a gate **insulator** which is polyimide and photo acryl. We investigated transfer and output characteristics of the thin film transistors having an active layer of pentacene. We calculated field effect mobility and on/off ratio from transfer characteristics of pentacene thin film transistor, and measured IR absorption spectrum of polyimide used as the gate **dielectric** layer. It was found that using the photo acryl as a gate **insulator** , threshold voltage decreased from -12.5 V to -7 V, field effect mobility increased from 0.012 cm/sup 2/ V/sup -1/ s/sup -1/ to 0.039 cm/sup 2/ V/sup -1/ s/sup -1/, and on/off current ratio increased from 10/sup 5/ to 10/sup 6/. It seems that TFTs using photo acryl gate **insulator** is more apt to form a channel than TFTs using polyimide gate **insulator**.

Subfile: B

37/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

6277108 INSPEC Abstract Number: B1999-08-2560R-003

Title: Process to fabricate high performance solid phase crystallized n-type and p-type thin film transistors on glass substrate

Author(s): Mourgues, K.; Raoult, F.; Helen, Y.; Mohammed-Brahim, T.; Rogel, R.; Bonnaud, O.

Author Affiliation: Rennes I Univ., France

Journal: Diffusion and Defect Data Part B (Solid State Phenomena)
Conference Title: Diffus. Defect Data B, Solid State Phenom. (Switzerland)
vol.67-68 p.547-51

Publisher: Balaban Publishers; Scitec Publications,

Publication Date: 1999 Country of Publication: Switzerland

CODEN: DDBPE8 ISSN: 1012-0394

SICI: 1012-0394(1999)67/68L.547:PFHP;1-E

Material Identity Number: B404-1999-003

Conference Title: Proceedings of the Fifth International Conference on Polycrystalline Semiconductors (POLYSE '98)

Conference Date: 13-18 Sept. 1998 Conference Location: Schwabisch Gmund, Germany

Language: English

Abstract: We have perfected a low thermal budget process (<600 degrees C) to fabricate high performance n and p type TFTs. They are elaborated in polycrystalline silicon on low cost glass substrates for active **matrix liquid crystal** display (AMLCD) applications.
Amorphous silicon layers are deposited by low pressure chemical vapor deposition (LPCVD) and subsequently solid phase crystallized. The flexibility of LPCVD with the control of the in-situ doping makes changes possible in the process. Indeed, this deposition technique allows the improvement of the polysilicon active layer/doped polysilicon layer interface. Drain and source regions are in-situ doped using phosphine for n type and diborane for p type transistors. The gate **insulator** is an atmospheric pressure chemical vapor deposited (APCVD) **SiO**/sub 2/ layer. The process does not include any hydrogenation step. This process allows the production of high TFTs with high characteristics uniformity on the whole substrate surface. Both n and p type TFT give high quality electrical properties: a high field effect mobility (mu /sub FEn/=100 cm/sup 2//Vs, mu /sub FEp/=60 cm/sup 2//Vs) and a low subthreshold slope (for both n and p type S=0.6 V/dec).

Subfile: B

37/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6006504 INSPEC Abstract Number: A9819-4280-002, B9810-4150D-016
Title: **Dielectric** properties of glass-dispersed liquid crystals
Author(s): Pena, J.M.S.; Olias, E.; Quintana, X.; Oton, J.M.
Author Affiliation: Area de Tecnologia Electronica, Univ. Carlos III, Madrid, Spain
Journal: Molecular Crystals and Liquid Crystals Conference Title: Mol. Cryst. Liq. Cryst. (Switzerland) vol.299 p.337-42
Publisher: Gordon & Breach,
Publication Date: 1997 Country of Publication: Switzerland
CODEN: MCLCE9 ISSN: 1058-725X
SICI: 1058-725X(1997)299L.337:DPGD;1-A
Material Identity Number: D151-98007
Conference Title: 16th International Liquid Crystal Conference
Conference Sponsor: ALCOM; Samsung Electron.; Gordon & Breach; Office of Naval Res.; et al
Conference Date: 24-28 June 1996 Conference Location: Kent, OH, USA
Language: English
Abstract: Liquid crystals can be dispersed in gel-glass **silica matrices** by sol-gel processes. The resulting gel-glass dispersed liquid crystals (GDLCs) are similar to polymer-dispersed liquid crystals; however, the use of an inorganic **silica matrix** yields a material with enhanced optical and mechanical properties. **Dielectric** properties of these materials are highly dependent on the manufacturing conditions. Impedance spectroscopy of the isolated **silica matrix** and the GDLC composite has been employed to characterize the system between 200 mHz and 8 MHz. The results have been compared to theoretical results based on several equivalent circuits.
Subfile: A B

37/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5972050 INSPEC Abstract Number: B9808-2560R-102
Title: A low temperature process (<or=600 degrees C) of unhydrogenated in-situ doped polysilicon thin film transistors for active **matrix** applications
Author(s): Pichon, L.; Raoult, F.; Mourgues, K.; Bonnaud, O.; Kis-Sion, K.
Author Affiliation: Groupe de Microelectron. et Visualisation, Rennes I Univ., France
Conference Title: ESSDERC'96. Proceedings of the 26th European Solid State Device Research Conference p.1059-62
Editor(s): Baccarani, G.; Rudan, M.
Publisher: Editions Frontieres, Gif-sur-Yvette, France
Publication Date: 1996 Country of Publication: France xliv+1107 pp.
ISBN: 2 86332 196 X Material Identity Number: XX97-01754
Conference Title: Proceedings of ESSDERC '96 - 1996 26th European Solid State Device Research Conference
Conference Date: 9-11 Sept. 1996 Conference Location: Bologna, Italy
Language: English
Abstract: Low temperature unhydrogenated in-situ doped polysilicon thin film transistors with a **SiO**/sub 2/ deposited gate **insulator** are elaborated through a four-mask aluminium process. The two polysilicon

layers, which constitute active layer and in-situ doped source and drain regions, are deposited at a pressure (P=90 Pa) in the amorphous state and crystallized by a thermal annealing. This last one is performed before plasma etching of the source/drain polysilicon layer. An oxygen plasma+RCA-type wet cleaning are ensured to obtain a good APCVD **SiO** /sub 2/ gate **insulator** /active layer interface quality. These thin film transistors exhibit very high electrical properties: a low threshold voltage (approximately=2 V), a high field effect mobility (>60 cm/sup 2//Vs), and a high On/Off state current ratio (>or=10/sup 7/) for a drain voltage V/sub ds/=1 V.
Subfile: B

37/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5967765 INSPEC Abstract Number: A9816-7865-056
Title: Nonlinear optical properties of modified DR1/**silica** films with highly ordered structures
Author(s): Young-Sun Cho; Kyung-Shin Min; Jae-Suk Lee; Gyoujin Cho; Kyeong Taek Jung; Yong Gun Shul; Wada, T.; Sasabe, H.
Author Affiliation: Dept. of Mater. Sci. & Eng., Kwangju Inst. of Sci. & Tech., South Korea
Journal: Molecular Crystals and Liquid Crystals Conference Title: Mol. Cryst. Liq. Cryst. (Switzerland) vol.294-295 p.263-6
Publisher: Gordon & Breach,
Publication Date: 1997 Country of Publication: Switzerland
CODEN: MCLCE9 ISSN: 1058-725X
SICI: 1058-725X(1997)294/295L.263:NOPM;1-5
Material Identity Number: D151-98004
Conference Title: First Asian Symposium on Organized Molecular Films for Electronics and Photonics (ASOMF'1)
Conference Date: 28-30 Oct. 1996 Conference Location: Ibaraki, Japan
Language: English
Abstract: Crosslinkable organic NLO chromophore (DRS) has been prepared and chemically incorporated into **silica matrices** using a sol-gel process. By monitoring the decay of UV absorbance as a function of time and temperatures, a number of electrically poled DRS/**silica matrix** systems have been investigated to elucidate the relaxation behaviors of the oriented organic chromophore by the poling. The value of the second order NLO coefficient d/sub 33/ was 47 pm/V for the DRS/**silica matrix** films with 0.4 mu m thickness. In addition, from the result of dramatic decreasing of UV absorbance after poling, it is speculated that the DRS may act as a liquid crystalline mesogenic groups and effectively oriented by the poling at the phase (nematic) transition temperature (80 degrees C) and locked in by the crosslinking. The crosslinking reactions between **silica matrices** and DRS chromophores have been proved using /sup 29/Si solid NMR measurement.
Subfile: A

37/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5919004 INSPEC Abstract Number: B9806-7260-171
Title: An RGB color VGA active-**matrix** EL display
Author(s): Aguilera, M.; Aitchison, B.; Basham, D.; Moehnke, S.; Ping, K.

; Tuenge, R.; Vetanen, W.; King, C.N.
Author Affiliation: Planar America, Beaverton, OR, USA
Conference Title: 1996 SID International Symposium. Digest of Technical Papers. First Edition p.125-8
Publisher: Soc. Inf. Display, Santa Ana, CA, USA
Publication Date: 1996 Country of Publication: USA xx+1022 pp.
Material Identity Number: XX96-00687
Conference Title: Proceedings of SID '96
Conference Date: 12-17 May 1996 Conference Location: San Diego, CA, USA
Language: English
Abstract: A color VGA active **matrix** electroluminescent (AMEL) display based on the broad band "white" EL phosphor and patterned color filters has been developed. The display utilizes the 24 micron pixel 1280*1024 AMEL design fabricated on single crystal silicon-on-**insulator** IC wafers. A wide color gamut is achieved using a quad arrangement of RGB color filter subpixels. A filtered white luminance of 40 fL is obtained at 3 kHz excitation.
Subfile: B

37/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5918940 INSPEC Abstract Number: B9806-7260-123
Title: Design of a high-density, gray scale, 1280*1024 active **matrix** EL (AMEL) display on SOI
Author(s): Hsueh, F.L.; Doiny, G.; Ipri, A.; Stewart, R.; Hsu, J.; Khormaei, R.; Rhoads, M.; Spitzer, M.; Keyser, T.; Becker, G.; Helgeson, M.; Nelson, S.
Author Affiliation: David Sarnoff Res. Center, Princeton, NJ, USA
Conference Title: Proceedings of Fifteenth International Display Research Conference. Asia Display '95 p.283-6
Publisher: Inst. Telev. Eng. Japan & SID, Tokyo, Japan & Santa Ana, CA, USA
Publication Date: 1995 Country of Publication: USA xxvi+981 pp.
Material Identity Number: XX95-01936
Conference Title: Proceedings of 15th International Display Research Conference
Conference Sponsor: Inst. Telev. Eng. Japan; SID
Conference Date: 16-18 Oct. 1995 Conference Location: Hamamatsu, Japan
Language: English
Abstract: For the first time, we describe the design of a high-density (1000 pixels per inch), gray scale, 1280*1024 active-**matrix** electroluminescent (AMEL) display using single-crystal silicon-on-**insulator** high-voltage IC technology. A pixel structure was designed to incorporate two MOS devices and an EL stack in the 24 mu m by 24 mu m area with minimal ac voltage noise. The peripheral input circuit architecture allows digital data to be written into the pixel array at greater than 1 GBS through 40 data inputs. The present AMEL display operates at 60 frames/second with an excitation voltage of 160 V at 3 kHz.
Subfile: B

37/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

5708834 INSPEC Abstract Number: A9721-6130-025
Title: **Dielectric** spectroscopy of nematic **liquid crystal** confined in random porous **matrices**
Author(s): Aliev, F.M.; Sinha, G.P.
Author Affiliation: Dept. of Phys., Puerto Rico Univ., San Juan, Puerto Rico
Conference Title: Electrically Based Microstructural Characterization. Symposium p.413-18
Editor(s): Gerhardt, R.A.; Taylor, S.R.; Garboczi, E.J.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1996 Country of Publication: USA xi+435 pp.
Material Identity Number: XX96-03176
Conference Title: Electrically Based Microstructural Characterization. Symposium
Conference Sponsor: Solartron Instrum.; Keithley Instrum.; NIST; NASA
Conference Date: 27-30 Nov. 1995 Conference Location: Boston, MA, USA
Language: English
Abstract: We performed **dielectric** spectroscopy measurements to study dynamics of dielectrically active modes of nematic liquid crystals (LC) 5CB with polar molecules confined in **silica** porous glasses with average pore sizes of 1000 AA (volume fraction of pores 40%) and 100 AA (27%). In the nematic phase of bulk 5CB there is only one mechanism of **dielectric** relaxation: rotation of polar molecules around short molecular axis with relaxation time tau ~10/sup -8/ s. The spatial confinement and the existence of a highly developed interphase have a strong influence on **dielectric** properties of LC. We found that at temperatures about 30 degrees C below the bulk melting point in both porous **matrices** the **dielectric** behavior of confined **liquid crystal** is very different from the behavior expected for solid state. The **dielectric** modes were not frozen in both porous **matrices** and we observed four well defined relaxational processes with relaxation times tau /sub 1/~10/sup -1/ s, tau /sub 2/~10/sup -5/ s, tau /sub 3/~10/sup -8/ s (bulk like) and tau /sub 3/~10/sup -9/ s. These four processes do not vanish even at temperatures corresponding to deep bulk isotropic phase. The relaxation time of the first process (slow) shows glass-like behavior in a wide temperature range below bulk melting point.
Subfile: A

37/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

5604539 INSPEC Abstract Number: B9707-7260-024
Title: Bonding techniques for single crystal TFT AMLCDs
Author(s): van der Groen, S.; Rosmeulen, M.; Jansen, P.; Deferm, L.; Baert, K.
Author Affiliation: IMEC, Leuven, Belgium
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2881 p.194-200
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1996 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2881L.194:BTSC;1-3
Material Identity Number: C574-96235
U.S. Copyright Clearance Center Code: 0 8194 2279 7/96/$6.00
Conference Title: Microelectronic Structures and MEMS for Optical Processing II
Conference Sponsor: SPIE; Semicond. Equipment & Mater. Int.; NIST

Conference Date: 14-15 Oct. 1996 Conference Location: Austin, TX, USA
Language: English
Abstract: Transmissive single crystal AMLCD light valves have recently drawn much attention for flat panel display applications. The active **matrix** circuits are fabricated on SIMOX wafers and then transferred to glass. Circuit transfer consists of bonding a CMOS processed SIMOX wafer to a Pyrex glass substrate, thinning the SIMOX wafer and opening the contact pads. The pixel electrodes are made in polysilicon to allow standard CMOS processing. This paper discusses the poly electrode transparency and evaluates the potential of anodic bonding and adhesive bonding for circuit transfer. A major challenge for anodic bonding is the protection of the device dielectrics from the high voltages applied during bonding. A test chip was designed to investigate different ways of circumventing breakdown of the dielectrics. A method for adhesive bonding is discussed that assures good uniformity of the thickness of the epoxy layer and avoids the inclusion of air bubbles. It is shown that the epoxies are resistant to the chemicals used for thinning the silicon substrate.
Subfile: B

37/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

5448905 INSPEC Abstract Number: B9701-7260-018
Title: Fabricating high resolution AMEL flat panel displays
Author(s): Aguilera, M.; Aitchison, B.
Author Affiliation: Planar Syst. Inc., Beaverton, OR, USA
Journal: Solid State Technology vol.39, no.11 p.109-10, 113-14, 116
Publisher: PennWell Publishing,
Publication Date: Nov. 1996 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
SICI: 0038-111X(199611)39:11L.109:FHRA;1-9
Material Identity Number: S046-96013
U.S. Copyright Clearance Center Code: 0038-111X/96/$1.00+.35
Language: English
Abstract: A new silicon-based design for active-**matrix** electroluminescent (AMEL) flat panel displays can achieve the high resolutions required for today's computer applications. The displays boast a dot pitch of only 24 mu m (>1000 lines/in) and resolutions of 640*480 and 1280*1024 pixels. Each pixel of a display needs its own addressing transistor, a data-field capacitor, and a high-voltage switching transistor. All row- and column-drivers are also located on the same chip. AMEL displays are fabricated using silicon-on-**insulator** (SOI) wafers with mostly standard CMOS processing. A refractory metal interconnect is needed to withstand the high temperatures and extended times required for the electroluminescent (EL)-film deposition process.
Subfile: B

37/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

5372911 INSPEC Abstract Number: B9610-7260-071
Title: Crystalline Si films for integrated active-**matrix** **liquid-crystal** displays
Author(s): Im, J.S.; Sposili, R.S.
Journal: MRS Bulletin vol.21, no.3 p.39-48

Publisher: Mater. Res. Soc,
Publication Date: March 1996 Country of Publication: USA
CODEN: MRSBEA ISSN: 0883-7694
SICI: 0883-7694(199603)21:3L.39:CFIA;1-4
Material Identity Number: M932-96004
Language: English
Abstract: The fabrication of thin-film-transistor (TFT) devices on a transparent glass substrate lies at the heart of active-**matrix-liquid crystal** -display (AMLCD) technology. It is possible to readily fabricate additional transistors to execute various electronic functions-those that would otherwise be handled by separate large-scale-integration (LSI) and very large-scale-integration (VLSI) circuits on the periphery of the display. Since this can be done, in principle, with no, or a minimal number of additional processing steps, substantial cost reduction is possible and significant value can be added to the final product. Doing so and doing it well can ultimately lead to "system-on-glass" products in which the entire electronic circuitry needed for a product is incorporated directly onto a glass substrate. This means that integrated active-**matrix liquid-crystal** displays (IAMLCDs) have the potential to bypass conventional Si wafer-based products and may lead TFT technology to compete directly against Si-wafer-based monolithic integrated circuits The authors discuss the technological issues involved.
Subfile: B

37/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

5351397 INSPEC Abstract Number: B9610-7260-021
Title: Silicon-on-quartz (SOQ) for high-resolution **liquid-crystal** light valves
Author(s): Sarma, K.R.; Rogers, C.; Chanley, C.
Author Affiliation: Honeywell Inc., Phoenix, AZ, USA
Conference Title: 1994 SID International Symposium Digest of Technical Papers. SID p.419-22
Editor(s): Morreale, J.
Publisher: SID, Santa Ana, CA, USA
Publication Date: 1994 Country of Publication: USA xviii+996 pp.
Material Identity Number: XX94-01147
Conference Title: Proceedings of SID '94 Symposium
Conference Date: 14-16 June 1994 Conference Location: San Jose, CA, USA
Language: English
Abstract: We developed a novel silicon-on-quartz (SOQ) approach for fabricating high mobility single crystal silicon transistors on transparent quartz substrates. Using this approach, we designed and fabricated a CMOS test chip and demonstrated SOQ test devices and circuits with a performance comparable to bulk single crystal silicon devices. The SOQ approach allows fabrication of the active **matrix** substrate with integrated row and column drivers for bright and compact, very high resolution **liquid crystal** light valve displays.
Subfile: B

37/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

5285741 INSPEC Abstract Number: B9607-7260-013
Title: Recent advances in fully-scanned active **matrix** displays using silicon-on-**insulator** technology
Author(s): Dolny, G.; Ipri, A.; Hsueh, F.; Stewart, R.; Atherton, J.; Cuomo, F.; Jose, D.; Spitzer, M.; Vu, D.P.; Batty, M.; Keyser, T.; Becker, G.; Khormaei, R.; Rhoades, R.; Tilton, M.; Ellis, R.; Franklin, H.; Helgeson, M.
Author Affiliation: David Sarnoff Res. Center, Princeton, NJ, USA
Conference Title: Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications p.426-33
Editor(s): Hunt, C.E.; Baumgart, H.; Iyer, S.S.; Abe, T.; Gosele, U.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1995 Country of Publication: USA vii+610 pp.
Material Identity Number: XX95-02968
Conference Title: Proceedings of Third International Symposium Semiconductor Wafer Bonding: Science, Technology and Applications
Conference Date: 21-26 May 1995 Conference Location: Reno, NV, USA
Language: English
Abstract: SOI technology is presently being used for the fabrication of both active **matrix liquid crystal** displays (AMLCD) and active **matrix** electroluminescent (AMEL) displays. It has unique advantages for the fabrication of flat panel displays, such as the production of devices with high performance and high breakdown voltage. It is the object of this paper to describe the technologies used for the fabrication of these displays and also to show the latest developments in these technologies.
Subfile: B

37/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

5056826 INSPEC Abstract Number: B9511-2570F-002
Title: The Kooi nitride effect revisited in TMOS HIPOX structures
Author(s): DeLoach, C.A.; Johnsen, B.; Omon, E.
Author Affiliation: CSPC, Motorola Inc., Phoenix, AZ, USA
Conference Title: ISTFA '94. Proceedings of the 20th International Symposium for Testing and Failure Analysis p.327-8
Publisher: ASM Int, Materials Park, OH, USA
Publication Date: 1994 Country of Publication: USA xiii+505 pp.
ISBN: 0 87170 543 5
Conference Title: Proceedings of 20th International Symposium for Testing and Failure Analysis
Conference Sponsor: ASM Int
Conference Date: 13-18 Nov. 1994 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: Summary form only given. TMOS is a vertical MOS structure called TMOS for the current flow through the device. The TMOS process flow consists of Si/sub 3/N/sub 4/ deposition and a high pressure oxidation (HIPOX) stage for field/isolation oxidation prior to gate oxide growth and polysilicon deposition. Gate oxide growth is preceded by a HIPOX etch to remove Si/sub 3/N/sub 4/ and HIPOX from the device active area. Standard MOS tests are implemented on TMOS devices. Voltage threshold, V/sub gs/, measures source drive time and channel concentration. Gate-source leakage current, IGSS, measures the gate oxide capability. A TMOS wafer line suffered poor yield for excessive IGSS. **Liquid crystal** analysis was used to identify the leakage current area as a rim along the active

area. Cross-sectional analysis and SIMS determined the root cause as oxide thinning near the active area edge or along the HIPOX beak edge. Further research indicated this is known as the Kooi nitride effect. The Kooi nitride effect is indicated by the mobility of water through the oxide during the HIPOX growth. If the water can combine with Si/sub 3/N/sub 4/ to form ammonia, the ammonia may move through the underlying Si/sub 3/N/sub 4/ and oxide to the Si surface, forming a parasitic Si/sub 3/N/sub 4/ layer, inhibiting gate oxide growth. A **matrix** of etch times were run in order to remove the nitride at the HIPOX etch and the IGSS failures were eliminated, improving the TMOS yield.
Subfile: B

37/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

4710272 INSPEC Abstract Number: B9408-7260-020
Title: Low temperature polysilicon TFTs for active **matrix** LCDs
Author(s): Pribat, D.; Plais, F.; Legagneux, P.; Kretz, T.; Stroh, R.; Huet, O.; Walaine, C.; Magis, M.; Jiang, N.; Hugon, M.C.; Agius, B.
Author Affiliation: Laboratoire Central de Recherches, Thomson-CSF, Velizy, France
Journal: Revue Technique Thomson-CSF vol.26, no.1 p.73-114
Publication Date: March 1994 Country of Publication: France
CODEN: RTTCBG ISSN: 0035-4279
Language: English
Abstract: An increasing proportion of the research and development effort which is devoted to active **matrix liquid crystal** displays is concentrated on polysilicon thin film transistor technology. The interest in polysilicon technology stems from the prospect of integrating the addressing and clocking circuitry at the periphery of the active plate, without additional cost. Early studies concerning the chemical vapor deposition of amorphous silicon were launched at the Laboratoire Central de Recherches (LCR) of THOMSON-CSF at the end of the seventies. The best amorphous precursor was obtained by pyrolysis of silane gas in low pressure chemical vapor deposition (LPCVD) conditions. In this paper, we describe amorphous silicon deposition and crystallization using a slightly different deposition technique: while keeping the basic LPCVD configuration and characteristics, our deposition chamber is inserted in an ultra high vacuum environment and the process gases are purified to several tens of ppb by point-of-use mineral getters or organic resins. This allows us to control impurity incorporation into the deposited films below ppm levels, particularly when disilane is used as gas precursor in replacement of silane. Moreover, we show that the use of disilane leads to the obtaining of very large grain sizes after isothermal crystallization at low temperature. We also introduce a novel plasma deposition technique, namely distributed electron cyclotron resonance (DECR)-plasma enhanced chemical vapor deposition (PECVD) which has allowed us to obtain device-grade **silicon dioxide** (for use as gate **dielectric**) without substrate heating.
Subfile: B

37/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

04332144 INSPEC Abstract Number: B9303-7260-017
Title: Polysilicon thin film transistor technology for active **matrix**

liquid crystal displays
Author(s): Chiang, A.
Author Affiliation: Xerox Palo Alto Res. Center, CA, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1815 p.128-38
Publication Date: 1992 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
U.S. Copyright Clearance Center Code: 0 8194 1015 2/92/$4.00
Conference Title: Display Technologies
Conference Sponsor: Nat. Chiao Tung Univ.; SPIE
Conference Date: 17-18 Dec. 1992 Conference Location: Hsinchu, Taiwan
Language: English
Abstract: As users demand higher quality in flat panel displays (FPD) with larger viewing areas and finer resolution, the polysilicon (p-Si) thin film transistor (TFTs) technology becomes increasingly important relative to the amorphous Si (a-Si) TFT technology employed in color active **matrix liquid crystal** displays (AMLCDs). The major advantages are its higher device speed and ability to integrate peripheral drivers with the display substrate, leading to higher panel performance and lower cost. The author first reviews the application and performance of p-Si TFT in AMLCDs. The development of TFT fabrication technology and the critical device characteristics governing the choices of processing techniques are then dealt with. The status of the manufacturing technology to realize low-cost high-performance TFT AMLCD is summarized.
Subfile: B

37/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

04068191 INSPEC Abstract Number: B9202-7260-045
Title: A study of poly-Si TFT **LCD** with very small pixel size and high aperture ratio
Author(s): Shimada, T.; Ueda, T.; Takafuji, Y.; Komiya, H.
Author Affiliation: LCD Group, Sharp Corp., Nara, Japan
Conference Title: Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials p.641-3
Publisher: Bus. Center Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1991 Country of Publication: Japan xvi+770 pp.
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE; Inst. Electron. Inf. Commun. Eng. Japan; et al
Conference Date: 27-29 Aug. 1991 Conference Location: Yokohama, Japan
Language: English
Abstract: Active **matrix LCD** with very small pixel size is discussed. A technique of making storage capacitor **dielectric** film thinner than TFT gate **dielectric** film is proposed to reduce the area of storage capacitor. This technique is applied to the fabrication of test panels with 37 mu m*32 mu m pixel size, using HTO film as gate and storage capacitor **dielectric** . Poly-Si TFTs with LDD structure are used as switching devices to reduce off-current. Drivers are fully integrated with CMOS configuration. Aperture ratio is 32%, and contrast ratio more than 50:1 is obtained.
Subfile: B

37/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

04045497 INSPEC Abstract Number: B9201-2570D-033

Title: Polycrystalline silicon thin-film CMOS technology: the poor man's SOI
Author(s): Ipri, A.C.; Dolny, G.; Policastro, S.; Stewart, R.; Peters, D.
Author Affiliation: David Sarnoff Res. Center, Princeton, NJ, USA
Conference Title: 1990 IEEE SOS/SOI Technology Conference. (Cat. No.90CH2891-0) p.113-14
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA vi+178 pp.
ISBN: 0 87942 573 3
U.S. Copyright Clearance Center Code: CH2891-0/90/0000-0113$01.00
Conference Sponsor: IEEE
Conference Date: 2-4 Oct. 1990 Conference Location: Key West, FL, USA
Language: English
Abstract: The authors discuss the electrical characteristics of thin film polycrystalline silicon transistors and their various uses. The first major application of polysilicon transistors was in the fabrication of active **matrix liquid crystal** displays. Over 40000 devices are fabricated on a four inch glass wafer and are used to make write only dynamic memory type full wafer arrays. The second major application of polysilicon transistors is as a replacement for the polysilicon load resistor in static memories. Future applications include circuits where both bulk silicon transistors and low performance silicon-on-**insulator** polysilicon transistors are used in the same integrated circuit. Typical of these applications are arrays where different substrate biases are needed and where junction isolation is insufficient for the application.
Subfile: B

37/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

03973843 INSPEC Abstract Number: B91062970
Title: Low temperature fabrication of high-mobility poly-Si TFTs
Author(s): Serikawa, T.; Shirai, S.; Okamoro, A.; Suyama, S.
Journal: NTT R & D vol.40, no.5 p.653-60
Publication Date: 1991 Country of Publication: Japan
CODEN: NTTDEC ISSN: 0915-2326
Language: Japanese
Abstract: A novel low temperature process has been proposed and developed for high-mobility polycrystalline silicon thin film transistors (poly-Si TFTs) to provide large-area high-resolution active **matrix liquid-crystal** displays at low cost. Its main feature is use of a sputter-deposited silicon film followed by laser irradiation and a gate **SiO** /sub 2/ film sputtered in an oxygen-argon mixture. The poly-Si TFTs have a mobility as high as 383 cm/sup 2//V.s, despite the small grain size of the poly-Si film. The poly-Si TFTs have been successfully applied to peripheral driver circuits for **liquid-crystal** displays.
Subfile: B

37/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

03275188 INSPEC Abstract Number: B89005579
Title: Improvement of electrical performance of CdSe TFTs for application to VFDs
Author(s): Shimojo, T.; Okada, S.; Kamogawa, H.; Kobayashi, M.
Author Affiliation: Ise Electron. Corp., Japan

Journal: Proceedings of the S.I.D vol.29, no.1 p.65-9
Publication Date: 1988 Country of Publication: USA
CODEN: SIDPAA ISSN: 0734-1768
U.S. Copyright Clearance Center Code: 0734-1768/88/2901-0065$1.00
Language: English
Abstract: Inverted staggered-type CdSe thin-film transistors (TFTs) with a **SiO** /sub 2/ overlay have been fabricated for application to vacuum fluorescent displays (VFDs). These exhibited good electrical performance and stability after two-step annealing; the first annealing was in air after deposition of the chromium source and drain, and the second in N/sub 2/ after deposition of the overlay. An ON/OFF current ratio exceeding 10/sup 4/ and a field-effect mobility ranging 80-140 cm/sup 2/ V/sup -1/ sec/sup -1/ could easily be obtained. Auger analysis for a CdSe channel of TFT samples having no **insulating** overlay revealed a difference in the surface composition between samples annealed in N/sub 2/ only and in the two-step annealing. The possibility of the TFT as an active **matrix** for VFD is examined.
Subfile: B

37/3,AB/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

03152252 INSPEC Abstract Number: B88039733
Title: A high-resolution active **matrix** using p-channel SOI TFTs
Author(s): Mimura, A.; Ohwada, J.-I.; Hosokawa, Y.; Suzuki, T.; Kawakami, H.; Miyata, K.
Author Affiliation: Hitachi Ltd., Ibaraki, Japan
Journal: IEEE Transactions on Electron Devices vol.35, no.4, pt.1 p.418-25
Publication Date: April 1988 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/88/0400-0418$01.00
Language: English
Abstract: A high-quality silicon-on-**insulator** (SOI) layer with 3-in-diameter quartz substrate and connected silicon islands was fabricated by a radio-frequency-heated zone-melting-recrystallization method. The whole area was successfully recrystallized and 95% of the silicon layer had a (100) surface. A p-channel thin-film transistor (TFT) with a mobility of 150-200 cm/sup 2//V-s and a high on-off ratio of 10/sup 6/ under illumination was fabricated. Using these TFTs, a high-resolution active **matrix** was fabricated and a high-contrast transmissive-type **liquid-crystal** display was achieved. Successful operation of logic circuits with the same frequency as the bulk devices indicated the possibility of monolithic driver integration.
Subfile: B

37/3,AB/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

03031268 INSPEC Abstract Number: B88004555
Title: **SiO**/sub x//TaO/sub x/ gate **insulator** a-Si TFT for **liquid crystal** displays
Author(s): Ikeda, M.; Dohjo, M.; Aoki, T.
Author Affiliation: Toshiba R&D Center, Kawasaki, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.26, no.9 p.1563-7
Publication Date: Sept. 1987 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922
Language: English
Abstract: A double layer of anodized TaO/sub x/ and plasma CVD **SiO** /sub x/ was applied to the gate **insulator** for an a-Si TFT active **matrix LCD** . This double layer was effective in eliminating interlayer short circuits between address bus lines and data bus lines in an **LCD** . No deterioration was observed in the TFT characteristics or the reliability upon adding a TaO/sub x/ layer to a **SiO**/sub x/ gate **insulator**. An **LCD** with no interlayer short circuits has been fabricated with this double layer.
Subfile: B

37/3,AB/24 (Item 24 from file: 2)
DIALOG(R)File 2:INSPEC

02109406 INSPEC Abstract Number: B83049301
Title: Materials limitations of amorphous-Si:H transistors (**liquid crystal** display addressing)
Author(s): Ast, D.G.
Author Affiliation: Materials Sci. & Engng. Dept., Cornell Univ., Ithaca, NY, USA
Journal: IEEE Transactions on Electron Devices vol.ED-30, no.5 p. 532-9
Publication Date: May 1983 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/83/0500-0532$01.00
Language: English
Abstract: Application of two-terminal (back-to-back diode) and three-terminal (FET) amorphous-Si:H devices to the **matrix** addressing of **liquid-crystal** displays (**LCD**) is discussed. a-Si:H back-to-back diodes appear to be suitable switching elements for displays of intermediate complexity. These devices are easy to fabricate and appear to have a high yield. An analysis of **matrix**-addressed LCDs shows that FETs implemented in a low-mobility material, such as a-$i:H, are best suited for (medium) high-resolution capacitorless displays where competing technologies (CdSe, poly-Si) are likely to encounter difficulties in meeting the off requirements. Instabilities in a-Si:H-based devices were studied by fabricating inverted and noninverted FETs with a variety of gate dielectrics: **SiO** /sub 2/, both thermally grown and sputtered; Si/sub 3/N/sub 4/ both by GD and LPCVD; and evaporated **SiO** /sub x/. Comparison of these devices, which are listed in decreasing order of stability, showed that a-Si:H FETs with thermal oxide were stable. In other devices, the decrease of the source-drain current I/sub SD/ with time was mainly caused by tapping at the semiconductor-**dielectric** interface.
Subfile: B

37/3,AB/25 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC

01935194 INSPEC Abstract Number: B82055713
Title: Stable thin-film transistors for **liquid-crystal matrix** displays
Author(s): Lee, M.J.; Wright, S.W.; Judge, C.P.
Author Affiliation: Electrical Engng. Dept., Imperial Coll., London, UK
Journal: Proceedings of the S.I.D vol.23, no.1 p.37-40
Publication Date: 1982 Country of Publication: USA
CODEN: SIDPAA ISSN: 0734-1768

Conference Title: Proceedings of the 1981 Society for Information Display International Symposium
Conference Date: 27 April-1 May 1981 Conference Location: New York, NY, USA
Language: English
Abstract: Thin-film transistors based on CdSe with **SiO**/sub 2/ as the **insulator** have been reproducibly prepared with decay rates which indicate less than 25% decay of drain current in six years of DC operation with gate fields of 5*10/sup 5/ V-cm/sup -1/. On:off ratios of 10/sup 5/-10/sup 6/ are readily achieved with off currents less than 6*10/sup -11/ amps per square. Devices show no significant change in electrical characteristics after operation at 100 degrees C in **liquid-crystal** material conditions or high humidity.
Subfile: B

37/3,AB/26 (Item 26 from file: 2)
DIALOG(R)File 2:INSPEC

01194369 INSPEC Abstract Number: A78043837, B78024385
Title: Electro-optical properties of nematic **liquid crystal** cell with pretilt angle
Author(s): Shimomura, T.; Mada, H.; Kobayashi, S.
Author Affiliation: Dept. of Visual Communication Design, Kyushu Inst. of Design, Fukuoka, Japan
Journal: Oyo Buturi vol.46, no.12 p.1179-85
Publication Date: Dec. 1977 Country of Publication: Japan
CODEN: OYBSA9 ISSN: 0369-8009
Language: Japanese
Abstract: The voltage and angular dependences of the transmittance of nematic **liquid crystal** cell with a pretilt angle have been studied both experimentally and theoretically from the physical aspects of color. The cell with a pretilt angle was made by rubbing or by slant evaporating **SiO** at an incident angle of 85 degrees from the substrate normal. The 4*4-**matrix** method by Berreman was used to determine the pretilt angle of nematic **liquid crystal** directors at the surface of the electrode. A nematic **liquid crystal** with a positive **dielectric** anisotropy (Delta epsilon >0) was used. Colorimetric data was shown on the UCS chromaticity diagram.
Subfile: A B

37/3,AB/27 (Item 27 from file: 2)
DIALOG(R)File 2:INSPEC

00981921 INSPEC Abstract Number: B76046979
Title: Thin film applications in flat image display panels
Author(s): Fischer, A.G.
Author Affiliation: Dept. of Electrical Engng., Thin Film Optoelectronics, Univ. of Dortmund, Dortmund, West Germany
Journal: Thin Solid Films vol.36, no.2 p.469-74
Publication Date: 2 Aug. 1976 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
Conference Title: 3rd International Conference on Thin Films
Conference Date: 25-29 Aug. 1975 Conference Location: Budapest, Hungary
Language: English
Abstract: The replacement of cathode ray tubes by flat panels is best achieved by using polycrystalline electroluminescent layers or twisted

nematic **liquid crystal** electrooptic layers which are electrically addressed by coextensive thin film transistor **matrices** in line-at-a-time fashion with elemental storage for the frame time. In order to facilitate automation, sets of fixed hole evaporation masks for 10000 elements, 15 cm*15 cm in size, have been developed. These are successively mated to the substrate. Obliquely evaporated **SiO** was used for TNLC molecule orientation. An electroluminescent powder specially treated for long life and embedded in the form of a monograin layer in a thermoplastic film of high **dielectric** constant was used to fabricate the EL layer on the TFT **matrix**. Contrast-enhancing back electrodes made of Al-Al/sub 2/O/sub 3/ cermet were developed.
Subfile: B

37/3,AB/28 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1461445 NTIS Accession Number: PB89-213789
Reports of the Research Laboratory, Asahi Glass Co., Ltd., Vol. 38, No. 2, 1988
Asahi Glass Co. Ltd., Yokohama (Japan). Research Lab.
Corp. Source Codes: 076427001
c1988 162p
Languages: Japanese
Journal Announcement: GRAI8922
Text in Japanese with English abstracts. See also PB89-213797 through PB89-213805 and PB89-156509.
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NTIS Prices: PC E07
Contents: Numerical simulation of viscoelastic flows using a penalty finite element model (in English); Properties of SiC-whisker reinforced glass-ceramic composite for biomedical application (in English); Ball impact damage of silicon carbide; Growth of MgO doped LiNbO3 single crystals; Preparation and properties of aromatic polysulfone/polythioethers ulfone copolymers; Analysis on fundamental properties of a perfluorinated carboxylate membrane by considering the distribution of electrolyte uptake inside the membrane; Transparent polyurethane elastomers--the influence of hard segment structure and content of its transparency and properties (in English); Determination of fluoropeptide sequence by secondary ion mass spectrometry; A new black/white dot **matrix LCD** (in English); Properties and applications of **silica** fiber by Sol-Gel process; Sound **insulation** performance of impact sound **insulating** floor system 'AS-Deck' for the detached house by wood construction; Characteristics of acousto-optic light switch module for distributed temperature sensor; **Liquid crystal** prompter.

37/3,AB/29 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04872939
E.I. No: EIP97113930692
Title: Plasma TEOS oxide for AMLCD manufacturing
Author: Law, K.; Robertson, R.; Blonigan, W.
Conference Title: Proceedings of the 1997 Display Manufacturing Technology Conference

Conference Location: San Jose, CA, USA Conference Date: 19970129-19970130
E.I. Conference No.: 47330
Source: Display Manufacturing Technology Conference, Digest of Technical Papers 1997. SID, Santa Ana, CA, USA. p 59
Publication Year: 1997
CODEN: 002724
Language: English
Abstract: Plasma TEOS oxide processes have been developed with AKT CVD equipment capable of depositing good quality **silicon dioxide** film uniformly over substrate area ranging from 300 mm multiplied by 400 mm to 550 mm multiplied by 650 mm. The unique chamber design allows efficient ionization of reactants and optimum reaction kinetics for both the gate **insulator** and interlayer **dielectric** (ILD) applications for polysilicon and amorphous silicon thin film transistor fabrication. The focus of process development was optimization of film properties such as thickness uniformity, morphology, step coverage and electrical characteristics. The challenge of providing a reliable TEOS delivery system suitable for high volume AMLCD production will be discussed. (Author abstract)

37/3,AB/30 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04200583
E.I. No: EIP95072765270
Title: Dynamics of ferroelectric and nematic liquid crystals confined in porous **matrices**
Author: Aliev, Fouad M.
Corporate Source: Univ of Puerto Rico, San Juan, PR, USA
Conference Title: Proceedings of the 1994 MRS Fall Meeting
Conference Location: Boston, MA, USA Conference Date: 19941128-19941201
E.I. Conference No.: 42888
Source: Dynamics in Small Confining Systems II Materials Research Society Symposium Proceedings v 366 1995. Materials Research Society, Pittsburgh, PA, USA. p 445-450
Publication Year: 1995
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Abstract: We performed **dielectric** spectroscopy measurements to study dynamics of collective modes of ferroelectric (FLC) and molecular motion of nematic (NLC) liquid crystals with polar molecules confined in **silica** macroporous and microporous glasses with average pore sizes of 1000 angstrom (volume fraction of pores 40%) and 100 angstrom (27%) respectively. For FLC the Goldstone and the soft modes are found in macropores. The rotational viscosity associated with the soft mode is about 10 times higher in pores than in the bulk. these modes are not detected in micropores although low frequency relaxation is present. The last one probably is not connected with the nature of **liquid crystal** but is associated with surface polarization effects typical for two component heterogeneous media. The difference between the dynamics of orientational motion of the polar molecules of NLC in confined geometries and in the bulk is qualitatively determined by the total energy F//s of the interaction between molecules and the surface of the pore wall, which is found F//s approximately equals 10**2 erg/cm**2. (Author abstract) 18 Refs.

37/3,AB/31 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03959443
E.I. No: EIP94101421048
Title: Liquid crystals - porous glasses heterogenous systems as materials for investigation of interfacial properties and finite-size effects
Author: Aliev, F.M.
Corporate Source: Kent State Univ, Kent, OH, USA
Source: Molecular Crystals and Liquid Crystals Science and Technology, Section A: Molecular Crystals and Liquid Crystals v 243 1994. p 91-105
Publication Year: 1994
CODEN: MCLCE9 ISSN: 1058-725X
Language: English
Abstract: Porous silicate glass can be used as an ideal **matrix** to study the influence of temperature on the surface effects that occur at the interface between the glass and some other material. Since the structural characteristics of these **matrices** are nearly independent of the temperature, all observable effects when the temperature is changed can be attributed to the change in the physical properties of the second component (LC). Moreover, the **dielectric** permittivity of **silica** porous glass **matrix** is independent of the temperature and frequency for a wide range of frequencies. This fact and the practically negligible electrical conductivity of the **matrix** greatly simplify the interpretation of the results and make it possible to avoid a number of difficulties that have been encountered earlier in studies of **dielectric** properties of heterogeneous systems. It is shown that micro-heterogenous systems which have a **liquid crystal** as one of the components (the other one is the porous glass) are useful materials for investigations of interfacial and finite-size phenomena in LC. The results on the structure and temperature dependence of the interfacial layer of 5CB at interface between LC and wall of pore as well as **dielectric** studies of the influence of confinement on dynamics of molecular motion of LC in pores are discussed. (Author abstract) 52 Refs.

37/3,AB/32 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03953784
E.I. No: EIP94101423366
Title: New fabrication technique for the integration of large area optoelectronic display panels
Author: Yeh, Hsi-Jen J.; Smith, John S.
Corporate Source: Univ of California, Berkeley, CA, USA
Conference Title: Proceedings of the Conference on Lasers and Electro-Optics
Conference Location: Anaheim, CA, USA Conference Date: 19940508-19940513
E.I. Conference No.: 20782
Source: Conference Proceedings - Lasers and Electro-Optics Society Annual Meeting v 8 1994. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA,94CH3463-7. p 191-192
Publication Year: 1994
CODEN: CPLSE4 ISBN: 0-7803-1971-0
Language: English
Abstract: A new technique for the integration of Si drivers on large-area active-**matrix** **LCD** display panels is proposed. Si driving circuitry is fabricated on silicon-on-**insulator** substrates. The drivers are separated by a mesa etch down to the **silicon** **dioxide** layer beneath the water surface. They are then lifted off the

Si substrate and are placed into an inert solution and flowed into holes made in a display panel to receive the devices. Electrical contacts are metallized on the panel to the drivers for each pixel. Finally, the **liquid crystal** layer is deposited and further processing is done to produce the large area display. With this technique, Si drivers can be fabricated densely packed on the available wafer area and are integrated on a panel with a much larger area. The size of the display is no longer limited by the size of the Si wafer.

37/3,AB/33 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518135
E.I. Monthly No: EI8802019455
Title: **SiO//x/TaO//x** **INSULATOR** a-Si TFT FOR **LIQUID CRYSTAL** DISPLAYS.
Author: Ikeda, Mitsushi; Dohjo, Masayuki; Aoki, Toshio
Corporate Source: Toshiba R&D Cent, Kawasaki, Jpn
Source: Jpn J Appl Phys Part 1 v 26 n 9 Sep 1987 p 1565-1567
Publication Year: 1987
CODEN: JAPNDE
Language: ENGLISH
Abstract: A double layer of anodized TaO//x and plasma CVD **SiO//x** was applied to the gate **insulator** for an a-Si TFT active **matrix** **LCD**. This double layer was effective in eliminating interlayer short circuits between address bus lines and data bus lines in an **LCD**. No deterioration was observed in the TFT characteristics or the reliability upon adding a TaO//x layer to a **SiO//x** gate **insulator**. An **LCD** with no interlayer short circuits has been fabricated with this double layer. (Author abstract) 4 refs.

37/3,AB/34 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02354308
E.I. Monthly No: EIM8711-080543
Title: CONSTRAINED FACET CRYSTAL GROWTH OF THIN FILMS ON AMORPHOUS SUBSTRATES.
Author: Aklufi, M.; Cadoff, I.
Corporate Source: US Naval Ocean Systems Cent, San Diego, CA, USA
Conference Title: Extended Abstracts - Fall Meeting (168th Society Meeting), the Electrochemical Society.
Conference Location: Las Vegas, NV, USA Conference Date: 19851013
E.I. Conference No.: 09038
Source: Electrochemical Society Extended Abstracts v 85-2. Publ by Electrochemical Soc, Pennington, NJ, USA p 638-639
Publication Year: 1985
CODEN: ESABB6 ISSN: 0160-4619
Language: English
Abstract: The usefulness of thin single crystal silicon films on electrically **insulating** substrates for electronic devices becomes apparent, when one considers that they are contained within the top micrometer of the silicon material. If the substrate is transparent it can, for large area **matrix** displays, support specific electronics that would accompany display mediums such as **liquid crystal** twist cells. Crystal growing from a single component melt, and its subsequent uncontrolled freezing results in a polycrystalline structure. However, it

has been shown for seeded crystal growth, freezing liquid-solid interfaces that are concave towards the liquid, favor single crystal growth. The crystallization of thin silicon films on amorphous **silicon dioxide** by laser shaped heat zones has been investigated, and is the subject of this paper. (Edited author abstract) 5 refs.

37/3,AB/35 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06335264 Genuine Article#: YK340 Number of References: 176
Title: Sol-gel methods for oxide coatings
Author(s): Francis LF
Corporate Source: UNIV MINNESOTA,DEPT CHEM ENGN & MAT SCI/MINNEAPOLIS//MN/55455
Journal: MATERIALS AND MANUFACTURING PROCESSES, 1997, V12, N6, P963-1015
ISSN: 1042-6914 Publication date: 19970000
Publisher: MARCEL DEKKER INC, 270 MADISON AVE, NEW YORK, NY 10016
Language: English Document Type: REVIEW

37/3,AB/36 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01529460 AAD9703554
PRODUCTION AND CHARACTERIZATION OF HIGH-QUALITY SOLID PHASE CRYSTALLIZED SILICON THIN FILMS ON **INSULATORS** (**LCD**)
Author: JUNG, SOON-MOON
Degree: PH.D.
Year: 1996
Corporate Source/Institution: UNIVERSITY OF FLORIDA (0070)
Source: VOLUME 57/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5849. 197 PAGES

Future active **matrix liquid crystal** displays (AMLCDs) require high performance thin film transistors (TFTs) on glass substrates in order to achieve high resolution, and fast response time. In this dissertation, a novel technique to produce large grained Si films on **insulators** at relatively low temperatures (below $600\sp\circ$C) has been developed. This method relies on the use of a single crystal Si wafer to initiate controlled nucleation and growth of crystalline silicon films from the amorphous phase. Detailed materials characterization has been conducted to understand the orientation, microstructure (grain sizes, defects, etc.), surface roughness, and nature of the nucleation phenomena.

For fabrication of crystalline Si films on **insulators**, amorphous Si was deposited on a **SiO**$\sb2$/Si substrate using LPCVD (low pressure chemical vapor deposition) at $540\sp\circ$C. The thickness of a-Si was varied from 300 to 1000A. The samples were furnace annealed at temperatures varying from 525 to $675\sp\circ$C. A single crystal Si wafer was used as a top seed to induce crystallization from the top surface of the a-Si film. The seeded and unseeded polycrystalline Si films were characterized using the techniques of differential reflectometry, transmission electron microscopy, X-ray diffraction, atomic force microscopy, and Hall measurements.

The origin of unseeded crystallization of a-Si film on **insulators** does not involve growth of pre-existing microcrystallites, but instead a random nucleation and growth process. The preferred orientation normal to the surface of grains was found to be $\langle111\rangle$ and the average grain size as found to be less than

0.2μm. The activation energies for nucleation and growth were determined to be 5.6 eV, and 3.7 eV, respectively, while the size of the critical nucleus was estimated to be $6.1\sim7.1\A.$
The top seeding technique produced very large $\langle110\rangle$ grain Si thin films on **insulators** when annealed at low temperatures and substantial short times. The transmission electron microscopy analysis showed that the crystallization of the films initiated from the top surface. However, these films showed also high density of twins and stacking faults. The preferred orientation of the films was found to be independent of the orientation of the top seed crystal. The Si self-ion implantation was found to increase the crystallization temperature. Hall mobility from these Si films (258 cm$\sp2$/Vsec) were found to be considerably larger than that of typical polycrystalline Si ${{\sim}10{\rm cm}\sp2/Vsec).$

37/3,AB/37 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

02963307 INSIDE CONFERENCE ITEM ID: CN031427217
The Improved Remote Plasma Scanning CVD for Gate **Insulator SiO** SUB 2 Films of Low Temperature Poly Silicon TFT **LCD**
Tanaka, J.; Saito, H.; Yoshizawa, T.; Okamoto, T.
CONFERENCE: Active-matrix liquid-crystal displays: TFT technologies and related materials-International workshop
INTERNATIONAL WORKSHOP ON ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS , 1999
P: 261-262
Tokyo, Japan Society of Applied Physics, 1999
LANGUAGE: English DOCUMENT TYPE: Conference Papers and programme
CONFERENCE SPONSOR: Japan Society of Applied Physics
CONFERENCE LOCATION: Tokyo
CONFERENCE DATE: Jul 1999 (199907) (199907)

37/3,AB/38 (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences

01689715 INSIDE CONFERENCE ITEM ID: CN017219179
Low Temperature Processed Poly-Si Thin Film Transistors with Thinner LPD-**SiO** SUB 2 as Gate **Insulator** and Its Reliability
Fan, C.-L.; Yeh, C.-F.; Tsai, H.-K.; Lur, W.
CONFERENCE: Active matrix liquid crystal displays: AMLCDs '95; second international workshop on active matrix liquid crystal displays-International workshop; 2nd
INTERNATIONAL WORKSHOP ON ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS , 1995; 2nd P: 93-96
IEEE, 1995
ISBN: 0780330560; 0780330579
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE SPONSOR: Lehigh University
IEEE Electron Devices Society
Society for Information Display
CONFERENCE LOCATION: Bethlehem, PA
CONFERENCE DATE: Sep 1995 (199509) (199509)
NOTE:
Described as proceedings. IEEE cat no 95TH8139

37/3,AB/39 (Item 3 from file: 65)

03/25/2003

DIALOG(R)File 65:Inside Conferences
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01523947 INSIDE CONFERENCE ITEM ID: CN015129548
Effect of Interface Treatment on the Performance of a-Si:H Thin Film Transistors with **SiO**~2 Gate **Insulator**
Kim, S. K.; Lee, K. S.; Kim, J. H.; Hong, C. H.
CONFERENCE: AM-LCD 94: 1994 International workshop on active matrix liquid crystal displays-International workshop
INTERNATIONAL WORKSHOP ON ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS , 1994
P: 12-15
Tokyo, BCAS, 1994
LANGUAGE: English DOCUMENT TYPE: Conference Papers and programme
CONFERENCE SPONSOR: Japan Society of Applied Physics
SID Japan Chapter
CONFERENCE LOCATION: Tokyo
CONFERENCE DATE: Nov 1994 (19941) (19941)

37/3,AB/40 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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05345549 JICST ACCESSION NUMBER: 03A0084012 FILE SEGMENT: JICST-E
Electro-Tunable Defect Mode in One-Dimensional Periodic Structure Containing Nematic **Liquid Crystal** as a Defect Layer.
OZAKI R (1); MATSUI T (1); OZAKI M (1); YOSHINO K (1)
(1) Osaka Univ., Osaka, Jpn
Jpn J Appl Phys Part 2, 2002, VOL.41,NO.12B, PAGE.L1482-L1484, FIG.4, REF.18
JOURNAL NUMBER: F0599BAD ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 535.374 544.252.22
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: Electrical tuning of defect modes in a one-dimensional periodic structure has been demonstrated using a nematic **liquid crystal** as a defect layer in the periodic structure. The wavelength of the defect mode shifts upon applying the electric field, which is due to the refractive index change in the defect layer caused by the field-induced realignment of the **liquid crystal** molecules. The theoretical calculation based on a simple transfer **matrix** has been carried out, and the result has been found to agree with the experimental result. (author abst.)

37/3,AB/41 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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02336743 JICST ACCESSION NUMBER: 95A0240239 FILE SEGMENT: JICST-E
Special issue : Material technology for **liquid crystal** device. Glass substrates for **liquid crystal** device.
ONODA TAKUHIRO (1)
(1) Nippon Electr. Co., Ltd.
Nyu Seramikkusu(New Ceramics), 1995, VOL.8,NO.3, PAGE.11-16, FIG.2, TBL.4, REF.5
JOURNAL NUMBER: L0595AAO ISSN NO: 0916-4057 CODEN: NYSEE
UNIVERSAL DECIMAL CLASSIFICATION: 666.5 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper explains alkaline elution, thermal dimentional stability, chemical resistance, surface quality, etc., as characteristics required for glass substrate for **liquid crystal** display (**LCD**).As glass substrates, it introduces glass for active **matrix LCD** and crystalline glass for color filter for p-Si AMLCD, and mentiones on future problems (enlargement in size and thinning).

37/3,AB/42 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01055106 JICST ACCESSION NUMBER: 90A0563188 FILE SEGMENT: JICST-E
Multi-color projection display using 3 ferro-electric **liquid crystal** light valves with 4 million pixels.
WAKITA NAOHIDE (1); IWAI YOSHIO (1); UEMURA TSUYOSHI (1); KIMURA SATOSHI (1); FUJIWARA SHOZO (1); GOHARA YOSHIHIRO (1); MASUMOTO YOSHIHIRO (1); MIYATAKE YOSHIHITO (1); OTA ISAO (1)
(1) Matsushita Electric Industrial Co., Ltd.
Terebijon Gakkaishi(Journal of the Institute of Television Engineers of Japan), 1990, VOL.44,NO.5, PAGE.525-530, FIG.10, TBL.2, REF.13
JOURNAL NUMBER: F0330ABG ISSN NO: 0386-6831
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: An high resolution, eight color, 38" projection display has been developed using three ferroelectric **liquid crystal** light valves (LVs) all with 2000*2000 pixels. Displays of high uniformity are attained by using the LVs developed with the ultra-fine precision processing technique and a high resolution optical system. The ultra high-resolution LVs (3.3" diagonal) with the pixel pitch of 30.MU.m (33lines/mm) are mounted with LSI driver chips assembled with the newly developed COG technology. The LV, filled with FLCs uniformly aligned by obliquely evaporated **SiO** layers with 2.0.MU.m spacing has excellent bistability and is addressed by a two slot multiplexing scheme of 1/2000 duty ratio. The display's contrast ratio is about 100:1 in a memorized state in the center area of the projection screen, in spite of the simplest structure which has no black-**matrix** layer. We successfully achieved molecular orientation causing black-**matrix** effect in the non-pixel areas by utilizing specially designed driving scheme (we call it "Field-Induced Black-**Matrix**"). This multi-color display with high contrast ratio and excellent color purity has and advantage over the laser addressing LC-LV system especially because its renewal speed is a few order faster. (author abst.)

37/3,AB/43 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00535563 JICST ACCESSION NUMBER: 88A0063664 FILE SEGMENT: JICST-E
SiOx/TaOx gate **insulator** a-Si TFT for **liquid crystal** displays.
IKEDA M (1); DOHJO M (1); AOKI T (1)

(1) Toshiba R&D Center, Kawasaki, JPN
Jpn J Appl Phys Part 1, 1987, VOL.26,NO.9, PAGE.1565-1567, FIG.3, REF.4
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3 621.385:621.397
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A double layer of anodized TaOx and plasma CVD SiOx was applied to the gate **insulator** for an a-Si TFT active **matrix** **LCD**. This double layer was effective in eliminating interlayer short circuits between address bus lines and data bus lines in an **LCD**. No deterioration was observed in the TFT characteristics or the reliability upon adding a TaOx layer to a SiOx gate **insulator** . An **LCD** with no interlayer short circuits has been fabricated with this double layer.(author abst.)

37/3,AB/44 (Item 5 from file: 94)

00418399 JICST ACCESSION NUMBER: 87A0255429 FILE SEGMENT: JICST-E
AC-field-stabilized **matrix** ferroelectric **LCD**.
WAKITA NAHOHIDE (1); UEMURA TSUYOSHI (1); ONISHI HIROYUKI (1); OTA ISAO (1)
(1) Matsushitadenkisangyo Musenken
Terebijon Gakkai Gijutsu Hokoku, 1987, VOL.10,NO.47, PAGE.13-18, FIG.14, REF.8
JOURNAL NUMBER: S0209AAF ISSN NO: 0386-4227
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

37/3,AB/45 (Item 1 from file: 144)

15653298 PASCAL No.: 02-0359014
Broadband **dielectric** spectroscopy of confined liquid crystals
Dielectric Spectroscopy
ALIEV F M; NAZARIO Z; SINHA G P
FELDMAN Yuri, ed; BERBERIAN John, ed; KREMER Friedrich, ed
Department of Physics, University of Puerto Rico, P.O. Box 23343, San Juan, PR 00931, United States; Department of Physics, CWRU, Cleveland, OH 44106, United States
The Hebrew University of Jerusalem, Givat Ram, Jerusalem, Israel; Saint Joseph's University, Philadelphia, PA, United States; Leipzig University, Leipzig, Germany
DS2001: International Dielectric Spectroscopy Conference, 1 (Jerusalem ISR) 2001-04-12
Journal: Journal of non-crystalline solids, 2002, 305 (1-3) 218-225
Language: English
Broad band **dielectric** spectroscopy has been applied for investigations of the dynamic behavior of **liquid crystal** 4-n-octyl-4'-cyanobiphenyl in the isotropic, nematic and smectic phases confined in porous **matrices** with randomly oriented, interconnected pores as well as in parallel cylindrical pores. The confinement strongly influences the dynamical behavior of LC and has resulted in qualitative

changes in their properties. The results on the influence of confinement on molecular relaxation due to reorientation of molecules around their short axis and librational motion are presented.

37/3,AB/46 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

14270384 PASCAL No.: 99-0474547
Transparent, high strain point spinel glass-ceramics
PINCKNEY L R
Corning Incorporated, SP-FR-5, Corning, NY 14831, United States
Journal: Journal of non-crystalline solids, 1999, 255 (2-3) 171-177
Language: English

Transparent, refractory glass-ceramics based on 10 nm crystals of spinel solid solution in a highly siliceous residual glass can be produced from compositions in the **SiO** SUB 2 -Al SUB 2 O SUB 3 -ZnO-MgO-TiO SUB 2 -ZrO SUB 2 system. The glass-ceramics possess excellent chemical durability as well as thermal expansion coefficients of 35-40x10 SUP - SUP 7 / Degree C and strain point temperatures of over 900 Degree C. Titania serves as both an extremely effective nucleating agent in these glasses and as an integral component of the spinel crystals. The materials are designed such that fluxes in the glass partition into the spinel crystals during the crystallization process, leaving a continuous residual glass very high in **silica** . The strain points of the resultant glass-ceramics approach those of vitreous **silica** and quartz materials which require significantly more expensive manufacturing processes. These glass-ceramics are excellent substrate candidates for high temperature, high quality polysilicon thin films. Potential products include solar cells and active **matrix liquid crystal** displays.

41/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14896355 PASCAL No.: 01-0044565
Image feature extraction with various wavelet functions in a photorefractive joint transform correlator
ZHANG H; CARTWRIGHT C M; DING M S; GILLESPIE W A
EPI Centre, University of Abertay Dundee, School of Science and Engineering, Bell Street, Dundee DD1 1HG, United Kingdom
Journal: Optics communications, 2000, 185 (4-6) 277-284
Language: English
The wavelet transform has found a lot of uses in the field of optics. We present an experimental realization of employing variant wavelet filters into the object space of a photorefractive joint transform correlator to realize image feature extraction. The Haar's wavelet, Roberts gradient and Mexican-hat wavelet are employed in the experiment. Because of its good optical properties, the photorefractive crystal Bi SUB 1 SUB 2 **SiO** SUB 2 SUB 0 is used as the dynamic holographic medium in the Fourier plane. Both scene and reference have been detour-phase encoded in a **liquid crystal** television in the input plane. Computer simulations, experimental results and analysis are presented.

41/3,AB/2 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

14451585 PASCAL No.: 00-0110552
Experimental implementation of a photorefractive joint transform correlator with circular harmonic filters
ZHANG H; CARTWRIGHT C M; DING M S; WANG Z Q; COOK N J; GILLESPIE W A
University of Abertay Dundee, School of Science and Engineering, Bell Street, Dundee, DD1 1HG, United Kingdom
Journal: Optics communications, 2000, 173 (1-6) 129-136
Language: English
We present an experimental realization of optical correlation for real-time rotational-invariance pattern recognition by means of a photorefractive joint transform correlator. Single and multiple circular harmonic components have been used to form correlation filters. The correlator operates with a **liquid crystal** television as the input images and a photorefractive crystal Bi SUB 1 SUB 2 **SiO** SUB 2 SUB 0 (BSO) as the recording medium. Suitable pre-processing of the references at the object plane makes up for the lack of light transmission. The properties of circular harmonic phase-only filter and circular harmonic matched filter have been compared. Also the noise robustness of these filters has been tested by tracking an object against a non-overlapping noise background. Analysis and experimental results are presented.

FILE 'WPIX, JAPIO'
L48 121 S L47
L49 1716 S (ZHANG H OR ZHANG, H OR ZHANG, HONGYONG OR ZHANG HONGYONG)/AU

FILE 'HCAPLUS'
L50 1121 S (ZHANG H OR ZHANG, H OR ZHANG, HONGYONG OR ZHANG HONGYONG)/AU
L51 1 S L50 AND (L11 OR L1 OR L6) AND (L2 OR L3 OR L12) AND L8

FILE 'DPCI'
L52 143 S (US20020055206 OR US5612254 OR US5504029 OR RE33829)/PN.G,PN.D

FILE 'WPIX, JAPIO'
L53 229699 S LCD OR LC(W) DISPLAY? OR LIQUID(W) CRYSTAL OR (U14-K01 OR W03-A08B OR W04-M01D3A OR T04-H03C2)/MC
L54 182522 S MATRIX OR MATRICES OR MATRIXES
L55 8270 S (MULTILEVEL OR MULTI(W) LEVEL OR MULTILAYER ? OR MULTI(W) LAYER)(4N)(INSULAT? OR DIELECTRIC)
L56 48997 S (SILICON)(W)(NITRIDE OR MONONITRIDE) OR SIN OR SI(W) N
L57 235023 S (SILICON)(W)(DIOXIDE OR MONOOXIDE) OR SIO OR SI(W) O OR SILICON(W) OXIDE OR SILICA
L58 71896 S GATE(W) ELECTRODE
L59 10308 S PIXEL(W) ELECTRODE
L60 32704 S (SOURCE OR DRAIN)(2N)(ELECTRODE)
L61 4233177 S CONTACT OR OPEN? OR VIA OR HOLE
L62 214227 S ETCH###
L63 3 S L53 AND L54 AND L55 AND L56
L64 90 S L53 AND L54 AND L57 AND L56
L65 29 S L64 AND L58
L66 20 S L64 AND L59
L67 21 S L64 AND L60
L68 25 S L64 AND L61
L69 16 S L64 AND L62
L70 63 S ((L65 OR L66 OR L67 OR L68 OR L69)) NOT L52
L71 63 S ((L65 OR L66 OR L67 OR L68 OR L69)) NOT L50
L72 105 S L49 AND L53
L73 5 S L72 AND L56 AND L57

L71 ANSWER 1 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2003-147634 [14] WPIX
DNN N2003-116586 DNC C2003-038046
TI Active-**matrix** substrate for **liquid-crystal** display devices comprises transparent dielectric base, and thin film transistors arranged near respective intersections of gate lines and data lines.
DC L03 P81 P85 U11 U12 U13
IN HIRATA, K
PA (NIDE) NEC CORP
CYC 3
PI US 2002149018 A1 20021017 (200314)* 21p
JP 2002268087 A 20020918 (200314) 9p
KR 2002073298 A 20020923 (200314)
ADT US 2002149018 A1 US 2002-95074 20020312; JP 2002268087 A JP 2001-70218 20010313; KR 2002073298 A KR 2002-13514 20020313
PRAI JP 2001-70218 20010313
AB US2002149018 A UPAB: 20030227
NOVELTY - An active-**matrix** substrate comprises:
(i) a transparent dielectric base;
(ii) gate lines arranged at intervals on the base;
(iii) data lines arranged to intersect with the gate lines;
(iv) thin film transistors arranged near the respective intersections of the gate and data lines;
(v) transparent dielectric portions arranged in a **matrix** array on the base;
(vi) planarization layer; and
(vii) **pixel electrodes**.
DETAILED DESCRIPTION - An active-**matrix** substrate comprises:
(a) a transparent dielectric base (1);
(b) gate lines arranged at intervals on the base;
(c) data lines arranged at intervals on the base to intersect with the gate lines, forming intersections;
(d) thin film transistors (TFTs) (2) arranged near the respective intersections of the gate and data lines;
(e) transparent dielectric portions (3a) arranged in a **matrix** array on the base in such a way as to form first recesses extending along the respective gate lines and second recesses (5b) extending along the respective data lines;
(f) planarization layer (6) selectively formed to fill the first and/or second recesses; and
(g) **pixel electrodes** (9) arranged on or over the flat surfaces of the respective portions.
Each of the dielectric portions forms pixel regions with a flat surface. Each has a thickness equal to or greater than a maximum height of the TFTs, the gate lines, or the data lines with respect to a specific reference level. Each has a distance equal to or greater than its thickness from a corresponding TFTs, gate lines, and/or data lines. Each of the **pixel electrodes** has a connection part (10) formed on the surface of the planarization layer to extend over a corresponding second recesses. The connection part is connected to corresponding TFTs by corresponding **holes** of the planarization layer.
An INDEPENDENT CLAIM is included for a method of fabricating an active-**matrix** substrate comprising
(1) providing a transparent dielectric base;
(2) forming TFTs, gate lines, and data lines on the base;
(3) forming a transparent dielectric layer on the base to cover the TFTs, the gate lines, and the data lines;

(4) selectively **etching** the transparent dielectric layer to form transparent dielectric portions on the base;

(5) selectively forming a planarization layer to fill at least the first and/or second recesses; and

(6) forming **pixel electrodes** arranged on or over the flat surfaces of the respective portions.

USE - For **liquid-crystal** display (**LCD**) devices.

ADVANTAGE - The active-**matrix** substrate suppresses effectively the unevenness of its surface due to the height difference of the thin film transistors (TFTs) and gate and data lines from the remaining area. It eliminates the difficulty in controlling the dimensional accuracy for the formation of the TFTs. It prevents the optical transmittance of the pixel regions from degrading due to the formation of the planarization layer in the pixel regions.

DESCRIPTION OF DRAWING(S) - The figure is a schematic, partial cross-sectional view, which shows a method of fabricating the active-**matrix** substrate.

Transparent glass plate 1

TFTs 2

Transparent dielectric portions 3a

Second recesses 5b

Planarization layer 6

Pixel electrodes 9

Connection part 10

Dwg.5D/7

L71 ANSWER 2 OF 63 WPIX (C) 2003 THOMSON DERWENT

AN 2003-016799 [01] WPIX

DNN N2003-012712 DNC C2003-004045

TI Thin film transistor for active **matrix** type **liquid crystal** display device, has **gate electrode**, gate insulating layer, semiconductor layer, **source** and **drain electrodes**, and passivation insulating layer.

DC L03 P81 P85 U11 U12 U14 V05

IN ANDO, M; KAWASAKI, M; WAKAGI, M

PA (HITA) HITACHI LTD; (ANDO-I) ANDO M; (KAWA-I) KAWASAKI M; (WAKA-I) WAKAGI M

CYC 2

PI US 2002117719 A1 20020829 (200301)* 16p

JP 2002252353 A 20020906 (200301) 10p

ADT US 2002117719 A1 US 2001-949846 20010912; JP 2002252353 A JP 2001-49982 20010226

PRAI JP 2001-49982 20010226

AB US2002117719 A UPAB: 20030101

NOVELTY - A thin film transistor comprises a **gate electrode**, a gate insulating layer, a semiconductor layer, a **drain electrode**, a **source electrode** and a passivation insulating layer which are formed in turn on an insulating substrate. A part of the gate insulating layer which is adjacent to the semiconductor layer is made of an oxide film.

DETAILED DESCRIPTION - A thin film transistor comprises a **gate electrode**, a gate insulating layer, a semiconductor layer, a **drain electrode**, a **source electrode** and a passivation insulating layer (19) which are formed in turn on an insulating substrate. A part of the gate insulating layer which is adjacent to the semiconductor layer is made of an oxide film. When a stress voltage is negative w.r.t to the **drain electrode** and the **source electrode** is applied to the **gate electrode**, an operating threshold voltage is reduced.

An INDEPENDENT CLAIM is included for the production of the above thin film transistor, comprising forming a first gate insulating layer made of **silicon nitride**, as a gate insulating layer on a **gate electrode** by utilizing plasma enhanced chemical vapor deposition; exposing a **silicon nitride** surface to an oxygen plasma to oxidize the **silicon nitride** surface to form a second gate insulating layer made of **silicon oxide** on the first insulating layer (13); and forming a silicon semiconductor film as a semiconductor layer (15) on the second insulating layer (14) by utilizing plasma enhanced chemical vapor deposition which is continuously implemented without breaking the vacuum.

USE - Used as a switching device in a display unit or a drive unit for an active **matrix** type display device (claimed).

ADVANTAGE - The transistor is capable of carrying out a stable switching operation.

DESCRIPTION OF DRAWING(S) - The figure is a vertical cross sectional view of a thin film transistor.

Substrates 11
Gate electrode 12
First insulating layer 13
Second insulating layer 14
Semiconductor layer 15
Source electrode 17
Drain electrode 18
Passivation insulating layer 19

Dwg.1/6

L71 ANSWER 3 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2002-488992 [52] WPIX
DNN N2002-386525
TI Array substrate for **LCD** device includes storage capacitors having specific electrode and **pixel electrode** together operating as one electrode and portion of gate line operating as other electrode.
DC P81 U11 U12 U14 W05
IN MUN, G H; MOON, K
PA (GLDS) LG PHILIPS LCD CO LTD
CYC 2
PI US 2002051099 A1 20020502 (200252)* 18p
KR 2002034272 A 20020509 (200272)
ADT US 2002051099 A1 US 2001-984257 20011029; KR 2002034272 A KR 2000-64379 20001031
PRAI KR 2000-64379 20001031
AB US2002051099 A UPAB: 20020815
NOVELTY - **Pixel electrodes** (117) formed at the intersections of several gate lines and data lines electrically **contacts** with **drain electrodes** (130) of TFT having gate insulating layers (133). Each storage capacitor has specific electrode (116) and **pixel electrode** together operating as one electrode and a portion (113a) of each gate line operating as other electrode (116).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for array substrate fabrication method.

USE - For active **matrix LCD** devices used in office automation equipments and video units.

ADVANTAGE - Capacitance of the storage capacitor is improved. Hence residual images in **LCD** are prevented from occurring and so manufacturing yield is increased.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of the array substrate.

Portion 113a

Pixel electrode 117
Drain electrode 130
Insulating layers 133
Electrode 116
Dwg.4k/4

L71 ANSWER 4 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2002-484579 [52] WPIX
CR 1996-084532 [09]
DNN N2002-382887 DNC C2002-138031
TI Thin film transistor for active **matrix** type **LCD** device, has silicon thin film containing oxygen, and specific amount of nitrogen concentration.
DC L03 P81 U11 U12 U14
PA (SEME) SEMICONDUCTOR ENERGY LAB
CYC 1
PI JP 2002134527 A 20020510 (200252)* 10p
ADT JP 2002134527 A Div ex JP 1994-151698 19940609, JP 2001-243010 19940609
PRAI JP 1994-151698 19940609; JP 2001-243010 19940609
AB JP2002134527 A UPAB: 20020815
NOVELTY - A **silicon nitride** membrane (102), active layers (103) and SiOxNy thin film (104), **silicon oxide** membrane (105) and **gate electrode** (106) are formed sequentially on a glass substrate (101). The nitrogen concentration in SiOxNy film, is 1 multiply 1015 - 1 multiply 1019 cm-3.
USE - For active **matrix** type **liquid crystal** display device.
ADVANTAGE - Thin film transistor with excellent electrical stability is obtained.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of thin film transistor, in various production process. (Drawing includes non-English language text).
Glass substrate 101
Silicon nitride membrane 102
Active layer 103
Thin film 104
Silicon oxide membrane 105
Glass substrate 106
Dwg.1/5

L71 ANSWER 5 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2002-319476 [36] WPIX
DNN N2002-250036 DNC C2002-092885
TI Active **matrix liquid-crystal** display for personal computer, has **silicon nitride** film which partially covers pixel **opening**.
DC A85 L03 P81 P85 U14
PA (SHAF) SHARP KK
CYC 1
PI JP 2001305583 A 20011031 (200236)* 7p
ADT JP 2001305583 A JP 2000-123238 20000424
PRAI JP 2000-123238 20000424
AB JP2001305583 A UPAB: 20020610
NOVELTY - Several polycrystalline silicon thin film transistors are laminated on a **silicon oxide** film formed on a TFT substrate (1). A **silicon nitride** film (9) is formed on the thin film transistor, such that it partially covers pixel **opening**.
USE - For personal computer.
ADVANTAGE - As the **silicon nitride** film partially covers the pixel **opening**, the interference of light in the pixel

opening due to difference of refractive index of each layer is prevented.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of active **matrix LC display** substrate.

TFT substrate 1

Silicon nitride film 9

Dwg.2/4

L71 ANSWER 6 OF 63 WPIX (C) 2003 THOMSON DERWENT

AN 2002-279739 [32] WPIX

DNN N2002-218408 DNC C2002-082237

TI Active **matrix liquid crystal** display device for in-plane switching system, comprises **liquid crystal** layer containing molecule of negative or positive dielectric anisotropy and dissociative dopant.

DC E14 L03 P81 P85 U11 U14 V07

IN IWAKABE, Y; KONDO, K; MATSUYAMA, S; OAKU, H; OHTA, M

PA (HITA) HITACHI LTD

CYC 3

PI US 2002004108 A1 20020110 (200232)* 39p

JP 2001354968 A 20011225 (200232) 26p

KR 2001112586 A 20011220 (200239)

ADT US 2002004108 A1 US 2001-866733 20010530; JP 2001354968 A JP 2000-173986 20000609; KR 2001112586 A KR 2001-31960 20010608

PRAI JP 2000-173986 20000609

AB US2002004108 A UPAB: 20020521

NOVELTY - An active **matrix liquid crystal** display device comprises a pair of substrates, a **liquid crystal** layer sandwiched by the substrates, orientation films, and a **pixel electrode** and a counter electrode. A **liquid crystal** molecule of the **liquid crystal** layer has negative or positive dielectric anisotropy. The **liquid crystal** layer contains a dopant having a dissociative group.

DETAILED DESCRIPTION - An active **matrix liquid crystal** display device comprises a pair of substrates, a **liquid crystal** layer sandwiched by the substrates, orientation films, and a **pixel electrode** (PX) and a counter electrode (CT) applying a voltage to the **liquid crystal** layer. The orientation films define an orientation direction of a **liquid crystal** molecule of the **liquid crystal** layer, and arranged between the substrates and the **liquid crystal** layer. The **liquid crystal** molecule has negative or positive dielectric anisotropy. The **liquid crystal** layer contains a dopant having a dissociative group.

USE - For use in twisted nematic display system or in-plane switching system.

ADVANTAGE - The inventive device maintains wide viewing angle characteristics, provides high quality display, and does not cause after image failure.

DESCRIPTION OF DRAWING(S) - The figure shows a plane view of the active **matrix** color **liquid crystal** display.

Counter voltage signal line CL

Counter electrode CT

Scanning signal line GL

Pixel electrode PX

Thin film transistors TFT

Dwg.1/21

L71 ANSWER 7 OF 63 WPIX (C) 2003 THOMSON DERWENT

AN 2002-239166 [29] WPIX
CR 2002-321683 [36]
DNN N2002-184417 DNC C2002-072063
TI **Liquid crystal** display unit includes pixels having first electrode(s) or wire(s) connected to corresponding one of scanning signal lines or corresponding one of video signal lines in pixels.
DC A85 A89 L03 P81 U14
IN ASHIZAWA, K; HIKIBA, M; ISHII, M; NAKAYAMA, T; OTA, M
PA (HITA) HITACHI LTD
CYC 2
PI US 2002008799 A1 20020124 (200229)* 121p
KR 2002005997 A 20020118 (200250)
ADT US 2002008799 A1 US 2001-899855 20010709; KR 2002005997 A KR 2001-41223 20010710
PRAI JP 2000-208587 20000710
AB US2002008799 A UPAB: 20020807
NOVELTY - A **liquid crystal** display unit includes pixels formed into a **matrix** on one of a pair of substrates by scanning signal lines and video signal lines. Each pixel includes first electrode(s) or wire(s) formed on a protective film. The first electrode(s) or wire(s) is connected to corresponding one of the scanning signal lines or corresponding one of the video signal lines in the pixels.

DETAILED DESCRIPTION - A **liquid crystal** display unit includes a **liquid crystal** layer held between a pair of substrates. Pixels are formed into a **matrix** on one of the substrates by scanning signal lines (GL) and video signal lines (DL). Each pixel includes a **pixel electrode** (PX) formed on one of the substrates. Each is supplied with a video signal from corresponding one of the video signal lines through a corresponding thin film transistor (TFT) on the basis of a scanning signal from corresponding one of the scanning signal lines. Opposed electrodes (CT, CT2) are formed on one of the substrates, and are supplied with an opposed voltage through an opposed voltage signal line (CL). A protective film is formed between the **liquid crystal** layer and a group of the scanning lines and/or a group of the video signal lines. A through **hole** (TH), which exposes the electrode(s) and lines to the **liquid crystal** layer, is formed onto the protective film. First electrode(s) or wire(s) (ST), which is connected to corresponding one of the scanning signal lines or corresponding one of the video signal lines in the pixels, is formed on the protective film. Second electrodes or wires, which are connected to a group of the **pixel electrodes**, a group of the opposed electrodes or a group of the opposed voltage signal lines, are formed on opposite sides of the first electrode or wire on the protective film.

USE - As a **liquid crystal** display unit.

ADVANTAGE - The **liquid crystal** display unit includes the first electrodes which can prevent or restrain the formation of black spot-like unevenness (small dark or white spots) when a current is supplied to the unit.

DESCRIPTION OF DRAWING(S) - The figure is a plan view showing one pixel in the **liquid crystal** display portion of an active-**matrix** type color **liquid crystal** display unit.

Opposed electrodes CT, CT2
Opposed voltage signal line CL
Video signal lines DL
Scanning signal lines GL
Pixel electrode PX
First electrode or wire ST
Thin film transistor TFT
Through **hole** TH

Dwg.1/86

L71 ANSWER 8 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2002-225615 [28] WPIX
DNN N2002-173037 DNC C2002-068705
TI Thin film semiconductor production comprises forming amorphous silicon film, introducing catalytic element to film, providing mask layer, forming sacrifice layer, introducing getter element, and performing heat treatment.
DC L03 U11 U13
IN FUKUSHIMA, Y
PA (SHAF) SHARP KK; (FUKU-I) FUKUSHIMA Y
CYC 3
PI US 2001041397 A1 20011115 (200228)* 9p
JP 2001319878 A 20011116 (200228) 8p
KR 2001104665 A 20011126 (200231)
ADT US 2001041397 A1 US 2001-847313 20010503; JP 2001319878 A JP 2000-138141 20000511; KR 2001104665 A KR 2001-25787 20010511
PRAI JP 2000-138141 20000511
AB US2001041397 A UPAB: 20020502
NOVELTY - A semiconductor is manufactured by forming an amorphous silicon film on a substrate, introducing into the film a catalytic element, providing a mask layer on a surface of the crystalline silicon film, forming a sacrifice layer, introducing a getter element, and performing a second heat treatment.

DETAILED DESCRIPTION - Manufacture of a semiconductor comprises forming an amorphous silicon film on a substrate (11), and introducing into the amorphous silicon film (12) a catalytic element for accelerating crystallization and performing a first heat treatment to crystallize the amorphous silicon film into a crystalline silicon film. A mask layer is provided having an **opening** extending thicknesswise on a surface of the crystalline silicon film, and a sacrifice layer is formed which continuously covers the surface of the mask layer and a portion of the crystalline silicon film corresponding to the **opening**. A gettering element for gettering the catalytic element is introduced to the sacrifice layer and the portion of the crystalline silicon film corresponding to the **opening**. A second heat treatment is performed to getter the catalytic element from the crystalline silicon film to the sacrifice layer through the **opening** of the mask layer.

USE - For manufacturing a silicon semiconductor thin film that is used for thin film transistors in active-**matrix** type **liquid crystal** displays.

ADVANTAGE - The method reduces catalytic element in a crystalline silicon film and increases the area of the crystalline silicon film to be left on the substrate. It also reduces catalytic-element concentration in the gettered region.

DESCRIPTION OF DRAWING(S) - The figure shows one step in the thin film transistor production.
Substrate 11
Amorphous silicon film 12
Dwg.1A/2

L71 ANSWER 9 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2002-065408 [09] WPIX
CR 2001-456594 [47]
DNN N2002-048568 DNC C2002-019256
TI **Liquid crystal** display device, e.g. active **matrix** display device used as video monitors, has dielectric material layer disposed over display electrodes and having **openings**, and **liquid crystal** material layer in

each **opening**.
DC A85 L03 P81 T04 U14
IN YANIV, Z
PA (YANI-I) YANIV Z
CYC 1
PI US 6262789 B1 20010717 (200209)* 9p
ADT US 6262789 B1 US 1998-200571 19981127
PRAI US 1998-200571 19981127
AB US 6262789 B UPAB: 20020208
NOVELTY - A **liquid crystal** display device having picture element(s) comprises a first display substrate having first and second major surfaces.

The substrate has display electrodes formed on one side of the major surfaces. A dielectric material layer is disposed over the display electrodes, and having **openings** formed over each display electrode. A **liquid crystal** material layer is positioned in each **opening**.

DETAILED DESCRIPTION - A **liquid crystal** display device having picture element(s) comprises a first display substrate having first and second major surfaces. The substrate has display electrodes (60, 62, 64) formed on one side of the major surfaces. A dielectric material layer (30) is disposed over the display electrodes, and having **openings** (32, 34, 36, 38, 40, 42, 44, 46, 48, 50) formed over each display electrode. A **liquid crystal** material layer is disposed in each **opening**. The picture element is defined by one of the display electrodes and the dielectric material layer formed over the corresponding display electrode.

USE - The **liquid crystal** display device, e.g. reflective display device, or active **matrix** display device (claimed) is used as video monitors in laptop computers, video cameras, and avionic navigation modules.

ADVANTAGE - The device is easy to manufacture, provides high manufacturing yields, demonstrate high reliability, and is low cost. It also provides full color, dynamic viewing angle, and present a low profile.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective cross sectional view from the side of a **liquid crystal** display device.

Dielectric material layer 30
Openings 32, 34, 36, 38, 40, 42, 44, 46, 48, 50
Display electrodes 60, 62, 64
Dwg.1/11

L71 ANSWER 10 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2001-540916 [60] WPIX
DNN N2001-402023 DNC C2001-161362
TI X-ray imaging device manufacture involves forming insulating layer between organic insulating layer and array of thin film transistors, which prevents organic insulating layer from directly contacting transistors.
DC A85 L03 P81 U11 U14
IN DEN BOER, W; GU, T
PA (BOER-I) DEN BOER W; (GUTT-I) GU T; (GUAR-N) GUARDIAN IND CORP
CYC 1
PI US 2001013908 A1 20010816 (200160)* 14p
US 6359672 B2 20020319 (200224)
ADT US 2001013908 A1 US 1997-954725 19971020; US 6359672 B2 US 1997-954725 19971020
PRAI US 1997-954725 19971020
AB US2001013908 A UPAB: 20011018
NOVELTY - An array of thin film transistors (TFTs) (9), an insulating layer (32), an organic polymer based insulating layer (33), and

contact holes (35) are sequentially formed on a substrate (19). An array of electrode members is formed on layer (33), so that electrode members in array are in communication with TFTs through **holes** (35). The layer (32) prevents layer (33) from directly contacting the TFTs.

DETAILED DESCRIPTION - The array of TFTs includes address lines connected to the TFTs.

INDEPENDENT CLAIMS are also included for the following:

(a) **liquid crystal** display manufacture; and

(b) TFT structure manufacture.

USE - The method is used for manufacturing an X-ray imaging device (claimed).

ADVANTAGE - An X-ray imaging device and an active **matrix liquid crystal** display having a high aperture ratio, are manufactured. The imaging device has an increased aperture ratio because the electrodes are formed on dual insulating layers so as to overlap portions of the array address lines and/or TFTs. Both the manufacturability and capacitive crosstalk of the device are improved due to the use of a photo-imageable organic insulating layer between **pixel electrodes** and address lines. An intermediate inorganic insulating layer is provided between the photo-imageable organic insulating layer and the overlapped TFTs, in order to prevent the organic insulating layer from directly contacting semiconductor material in the TFTs, thereby reducing potential voltage swings.

DESCRIPTION OF DRAWING(S) - The figure shows the side elevational cross-sectional view of TFT array manufacture.

Thin film transistors 9

Substrate 19

Insulating layers 32, 33

Contact holes 35

Dwg.7/7

L71 ANSWER 11 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2001-483098 [52] WPIX
DNN N2001-357605 DNC C2001-144809
TI Production of top gate thin-film transistors used in flat panel displays involves laser annealing amorphous silicon layer not shielded by gate conductor through all gate insulator layers to form polycrystalline silicon portions.
DC L03 U11 U12 U14
IN GLASSE, C; MCCULLOCH, D J
PA (PHIG) US PHILIPS CORP; (PHIG) KONINK PHILIPS ELECTRONICS NV
CYC 22
PI WO 2001052313 A1 20010719 (200152)* EN 27p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP
US 2001026962 A1 20011004 (200161)
EP 1166348 A1 20020102 (200209) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
ADT WO 2001052313 A1 WO 2000-EP13221 20001227; US 2001026962 A1 US 2001-754180 20010103; EP 1166348 A1 EP 2000-990023 20001227, WO 2000-EP13221 20001227
FDT EP 1166348 A1 Based on WO 200152313
PRAI GB 2000-292 20000107
AB WO 200152313 A UPAB: 20010914
NOVELTY - A top gate thin-film transistor is produced by laser annealing amorphous silicon layer not shielded by the gate conductor, through all of the gate insulator layers, to form polycrystalline silicon portions.

DETAILED DESCRIPTION - Production of a top gate thin film transistor comprises:

(a) forming an amorphous silicon layer (12) over an insulating substrate (2);

(b) forming an insulated gate structure over the amorphous silicon layer comprising gate insulator layers (14a, 14b) and an upper gate conductor directly over the gate insulator layers;

(c) laser annealing areas of the amorphous silicon layer not shielded by the gate conductor (16), through all of the gate insulator layers, to form polycrystalline silicon portions.

The gate conductor is patterned to be narrower than a spacing to be provided between **source** and **drain electrode** (6, 8) **contacts** to the silicon layer. The gate insulator layers are formed as a gate insulator layer of first refractive index, and an overlying surface insulator layer (14c) of second, lower, refractive index.

An INDEPENDENT CLAIM is also included for a top gate thin-film transistor.

USE - The method is used for producing top gate thin-film transistor useful in flat panel display devices, e.g., active-**matrix liquid-crystal** displays or other large-area electronic devices.

ADVANTAGE - The overlying surface insulator layer has been found to reduce fluctuations in the reflectance of the structure in dependence upon the specific thickness of the gate insulator layers. Thus, the tolerances for the thickness of the gate insulator layers are avoided whilst maintaining control of the laser annealing process. Since, the laser annealing is performed through all of the gate insulator layers, additional **etching** steps are no longer required.

DESCRIPTION OF DRAWING(S) - The figure shows a thin-film transistor configuration.

Insulating substrate 2

Source/drain electrode 6, 8

Impurity atoms 10

Silicon layer 12

Gate insulator layers 14a, 14b

Surface insulator layer 14c

Gate conductor 16

Dwg.3/7

L71 ANSWER 12 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2001-255031 [26] WPIX
CR 2001-189746 [19]
DNN N2001-195679 DNC C2001-083154
TI Manufacture of thin film transistor by depositing amorphous silicon on substrate and patterning to form active layer, heavily doping impurities in active layer, and converting active layer of amorphous silicon to polysilicon.
DC L03 U11 U12 U14
IN LEE, J H; LEE, S G; LEE, S; YI, J
PA (GLDS) LG PHILIPS LCD CO LTD
CYC 2
PI KR 2000061176 A 20001016 (200126)*
US 6207481 B1 20010327 (200129)B 19p
KR 317622 B 20011222 (200250)
ADT KR 2000061176 A KR 1999-10051 19990324; US 6207481 B1 US 1999-458468 19991209; KR 317622 B KR 1999-10051 19990324
FDT KR 317622 B Previous Publ. KR 2000061176
PRAI KR 1999-10051 19990324
AB US 6207481 B UPAB: 20010528 ABEQ treated as Basic

NOVELTY - A thin film transistor is manufactured by depositing amorphous silicon on substrate and patterning the deposited amorphous silicon to form an active layer, heavily doping impurities in the active layer using **gate electrode** as mask to form source and drain region in the active layer, and converting active layer from amorphous silicon to

polysilicon through metal induced crystallization process.

DETAILED DESCRIPTION - Manufacture of thin film transistor involves depositing amorphous silicon on a substrate and patterning to form an active layer (218). A block layer is formed centrally located on the active layer to function as mask during an impurity doping process so that a channel region is defined in an approximately central portion in the active layer. An exposed surface of the active layer is silicidized to form a crystallization seed layer (224), and the block layer is then removed. A gate insulating layer (226) is formed on the substrate to cover the active layer and the crystallization seed layer. A **gate electrode** (228) is defined on the gate insulating layer so that the **gate electrode** is located on a portion which corresponds to the channel region of the active layer, with the **gate electrode** overlapping with a portion of the crystallization seed layer. The active layer is heavily doped with impurities using the **gate electrode** as a mask to form source and drain regions (230, 231) in the active layer from amorphous silicon to polysilicon through a metal induced lateral crystallization process caused by the crystallization seed layer.

USE - For manufacturing a thin film transistor used as switching devices for a pixel block and driving devices for a driver circuit block in an active **matrix** type **liquid crystal** display.

ADVANTAGE - The active layer is formed of polysilicon providing crystals, which are uniform in size, making the electrical properties of the resulting transistor uniform. The source and drain regions are not in direct **contact** with first and second interconnecting layers so that oxidation of the source and drain regions is avoided to prevent the **contact** resistance from increasing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a process for manufacturing the thin film transistor.

Active layer 218

Crystallization seed layer 224

Gate insulating layer 226

Gate electrode 228

Source and drain regions 230, 231

Dwg.6E/7

AB KR2000061176 A UPAB: 20020807

NOVELTY - A thin film transistor is manufactured by depositing amorphous silicon on substrate and patterning the deposited amorphous silicon to form an active layer, heavily doping impurities in the active layer using **gate electrode** as mask to form source and drain region in the active layer, and converting active layer from amorphous silicon to polysilicon through metal induced crystallization process.

DETAILED DESCRIPTION - Manufacture of thin film transistor involves depositing amorphous silicon on a substrate and patterning to form an active layer (218). A block layer is formed centrally located on the active layer to function as mask during an impurity doping process so that a channel region is defined in an approximately central portion in the active layer. An exposed surface of the active layer is silicidized to form a crystallization seed layer (224), and the block layer is then removed. A gate insulating layer (226) is formed on the substrate to cover the active layer and the crystallization seed layer. A **gate electrode** (228) is defined on the gate insulating layer so that the **gate electrode** is located on a portion which corresponds to the channel region of the active layer, with the **gate electrode** overlapping with a portion of the crystallization seed layer. The active layer is heavily doped with impurities using the **gate electrode** as a mask to form source and drain regions (230, 231) in the active layer from amorphous silicon to polysilicon through a metal induced lateral crystallization

process caused by the crystallization seed layer.

USE - For manufacturing a thin film transistor used as switching devices for a pixel block and driving devices for a driver circuit block in an active **matrix** type **liquid crystal** display.

ADVANTAGE - The active layer is formed of polysilicon providing crystals, which are uniform in size, making the electrical properties of the resulting transistor uniform. The source and drain regions are not in direct **contact** with first and second interconnecting layers so that oxidation of the source and drain regions is avoided to prevent the **contact** resistance from increasing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a process for manufacturing the thin film transistor.

Active layer 218

Crystallization seed layer 224

Gate insulating layer 226

Gate electrode 228

Source and drain regions 230, 231

Dwg.6E/7

L71 ANSWER 13 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2001-052430 [07] WPIX
CR 1997-539263 [50]
DNN N2001-040359 DNC C2001-014602
TI Active **matrix liquid crystal** display manufacture involves removing passivation layer whose edges are aligned with that of semiconductor and insulating layers to form **contact holes** exposing **drain electrodes**.
DC A14 A28 A85 L03 P81 U11 U14
IN AN, B; HAN, C; KIM, J H; LIM, K N; LYU, K
PA (GLDS) LG ELECTRONICS INC
CYC 1
PI GB 2350467 A 20001129 (200107)* 26p
GB 2350467 B 20010411 (200122)
ADT GB 2350467 A Derived from GB 1997-10603 19970522, GB 2000-20848 20000823;
GB 2350467 B Derived from GB 1997-10603 19970522, GB 2000-20848 20000823
PRAI KR 1996-17813 19960523
AB GB 2350467 A UPAB: 20010421

NOVELTY - Passivation layer (113a) is formed covering gate insulating layer (109), semiconductor layer (111) and ohmic **contact** layer (112) formed on substrate (110). Layers (113a, 111, 109) are **etched** so that their edges are aligned suitably. Layer (113a) is selectively removed to form **contact holes** exposing **drain electrodes** (106). **Pixel electrodes** are formed on **drain electrodes** and passivation layer.

DETAILED DESCRIPTION - The method of forming an active **matrix liquid crystal** display involves forming gate bus lines (117) and **gate electrodes** (107) on a substrate (110). A gate insulating layer (109), semiconductor layer (111) and ohmic **contact** layer (112) are sequentially formed on gate bus lines, the **gate electrodes** and the substrate. Source bus lines, **source electrodes** (105) and **drain electrodes** (106) are formed on the ohmic **contact** layer. A passivation layer (113a) is formed covering the semiconductor layer, source bus lines, **source** and **drain electrodes** . The passivation layer, the semiconductor layer and the gate insulating layer are **etched** so that their edges are substantially aligned. The passivation layers is removed selectively to form **contact holes** which expose **drain electrodes**. **Pixel electrodes** are formed on the **drain**

electrode and the passivation layer.

An INDEPENDENT CLAIM is also included for active **matrix liquid crystal** display.

USE - None given.

ADVANTAGE - By selective coating of organic material on the passivation layer, level difference does not exists on the surface of passivation layer, thereby enabling uniform formation of **pixel electrodes**. The aperture ratio of **LCD** can be improved by minimizing defects in rubbing as level difference does not exist on the passivation layer. **LCD** manufacturing yield is improved as patterning process can be reduced remarkably.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of AMLCD manufacturing method.

Electrodes 105,106

Gate electrodes 107

Gate insulating layer 109

Substrate 110

Semiconductor layer 111

Ohmic **contact** layer 112

Passivation layer 113a

Gate bus lines 117

Storage capacitor electrodes 130

Dwg.5F/6

L71 ANSWER 14 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2000-285863 [25] WPIX
CR 1997-477483 [44]; 2000-368919 [27]
DNN N2000-215304 DNC C2000-086533
TI Thin film transistor for active **matrix liquid crystal** display, includes insulation film comprising laminated layers of **silicon nitride** or **silicon oxide**.
DC L03 P81 P85 U12 U14
PA (SEME) SEMICONDUCTOR ENERGY LAB
CYC 1
PI JP 2000077677 A 20000314 (200025)* 11p
ADT JP 2000077677 A Div ex JP 1996-352962 19961213, JP 1999-230989 19961213
PRAI JP 1995-347754 19951214
AB JP2000077677 A UPAB: 20000706

NOVELTY - Over a substrate a **gate electrode**, a gate insulation film, a silicon film, a layer insulation film and a resin layer are formed sequentially. The layer insulation film includes laminated layers of **silicon nitride**, oxidation **silicon nitride** or **silicon nitride** and **silicon oxide**.

USE - For active **matrix**, **LCD**, EL type display.

ADVANTAGE - Prevents water or dust penetration due to layer insulation film. Reduces capacitance formation between thin film transistor and **pixel electrode** and wiring and offers inexpensive component with high productivity.

DESCRIPTION OF DRAWING(S) - The figure explains the production process of thin film transistor.

Dwg.6/6

L71 ANSWER 15 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 2000-259236 [23] WPIX
DNN N2000-192864 DNC C2000-079463
TI Apparatus having integrated circuits made of thin film transistor devices has second insulating film and semiconductor film formed successively without exposure to the atmosphere.
DC L03 U11 U12 U14

IN KASAHARA, K
PA (SEME) SEL SEMICONDUCTOR ENERGY LAB; (SEME) SEMICONDUCTOR ENERGY LAB
CYC 26
PI EP 993032 A2 20000412 (200023)* EN 30p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000183360 A 20000630 (200037) 26p
ADT EP 993032 A2 EP 1999-119516 19991001; JP 2000183360 A JP 1999-274106 19990928
PRAI JP 1998-283711 19981006
AB EP 993032 A UPAB: 20000516
NOVELTY - Device includes first insulating layer on a substrate and heat-treated, second insulating film on the first insulating film, and semiconductor film on the second insulating film. The second insulating and semiconductor films are formed successively without exposure to the atmosphere. Hence the interface between an active layer, particularly a channel forming region, and a base film is improved.

DETAILED DESCRIPTION - The semiconductor device includes:

(a) a 100-500 nm thick first insulating film formed over a substrate;

(b) a 10-100 second insulating film in **contact** with the first insulating film;

(c) a channel-forming region and source and drain regions formed on both sides of the channel forming region which is formed in **contact** with the second insulating film;

(d) a gate insulating layer in **contact** with the channel forming region; and

(e) a gate line provided over the channel forming region with the gate insulating layer interposed between them.

The impurity concentration in the layer at the interface between the first and second insulating films is higher than that in an interface between the second insulating film and the channel forming region.

A low concentration impurity region is formed between the channel; forming region and the source region or between the channel forming region and the drain region.

The second insulating film and the channel forming region are formed by successive formation in laminated layers without exposure to the atmosphere.

A catalytic element that accelerates crystallization of silicon is contained in at least the source region and the drain regions.

INDEPENDENT CLAIMS are given for methods of manufacturing a semiconductor device, where the first insulating film is heat-treated at 200-700 deg. C.

USE - For semiconductor apparatus such as thin film transistors (TFT) and MOS transistors, and also displays and electrooptic apparatus, such as image sensors.

ADVANTAGE - Improved interface between an active layer, particularly a channel forming layer, and a base film to improve ,e.g., TFT characteristics. High reliability of semiconductor device.

DESCRIPTION OF DRAWING(S) - The device shows the construction of a semiconductor apparatus (**liquid crystal** display).

Glass substrate 500
Pixel **matrix** circuit 501
Scan line drive circuit 502
Signal line drive circuit 503
Flexible printed circuit 510
IC chip 511, 512
Logic circuit 520
Counter substrate 530
Dwg.5/17

L71 ANSWER 16 OF 63 WPIX (C) 2003 THOMSON DERWENT

AN 2000-220951 [19] WPIX
DNN N2002-118067 DNC C2002-048622
TI In-plane switching mode **liquid crystal** display device comprises first and second substrates, gate and data bus lines, common line, pair of first and second electrodes, and **liquid crystal** layer.
DC A85 L03 P81 U12 U14
IN HAM, Y; HAHM, Y S; HAM, Y S
PA (GLDS) LG PHILIPS LCD CO LTD; (GLDS) LG ELECTRONICS INC; (HAMY-I) HAM Y S
CYC 2
PI KR 99016341 A 19990305 (200019)*
KR 255931 B1 20000501 (200128)
US 2001046018 A1 20011129 (200221)B 7p
ADT KR 99016341 A KR 1997-38863 19970814; KR 255931 B1 KR 1997-38863 19970814; US 2001046018 A1 US 1998-134405 19980814
PRAI KR 1997-38863 19970814
AB US2001046018 A UPAB: 20020403 ABEQ treated as Basic
NOVELTY - An in-plane switching mode **liquid crystal** display device comprises: first and second substrates; gate and data bus lines defining pixel regions and arranged on the first substrate; common line in the pixel regions; pair of first and second electrodes parallel to each other applying plane electric fields in the pixel regions; and **liquid crystal** layer between first and second substrates.

DETAILED DESCRIPTION - An in-plane switching mode **liquid crystal** display device comprises: first and second substrates; gate and data bus lines defining pixel regions and arranged on the first substrate; common line in the pixel regions; pair of first and second electrodes parallel to each other applying plane electric fields in the pixel regions; and **liquid crystal** layer between first and second substrates. d Delta n is 0.29-0.36 mu m, where d is the thickness of the **liquid crystal** layer, and Delta n is the refractive anisotropy of the **liquid crystal** molecule.

An INDEPENDENT CLAIM is also included for a method of making an in-plane switching mode (**LCD**) device having first and second substrates comprising:

(a) forming gate and data bus lines defining pixel regions and arranged on the first substrate;

(b) forming a common line in the pixel regions;

(c) forming a pair of first and second electrodes parallel to each other, applying plane electric fields in the pixel regions; and

(d) forming a **liquid crystal** layer between the first and second substrates.

USE - None given.

ADVANTAGE - The in-plane switching mode **liquid crystal** display (**LCD**) device has high light transmittance by controlling the refractive anisotropy of the **liquid crystal** molecule and the thickness of the **liquid crystal** layer. The **LCD** prevents color-shift.

Dwg.0/3

AB KR 99016341 A UPAB: 20020409
NOVELTY - An in-plane switching mode **liquid crystal** display device comprises: first and second substrates; gate and data bus lines defining pixel regions and arranged on the first substrate; common line in the pixel regions; pair of first and second electrodes parallel to each other applying plane electric fields in the pixel regions; and **liquid crystal** layer between first and second substrates.

DETAILED DESCRIPTION - An in-plane switching mode **liquid**

crystal display device comprises: first and second substrates; gate and data bus lines defining pixel regions and arranged on the first substrate; common line in the pixel regions; pair of first and second electrodes parallel to each other applying plane electric fields in the pixel regions; and **liquid crystal** layer between first and second substrates. d Delta n is 0.29-0.36 mu m, where d is the thickness of the **liquid crystal** layer, and Delta n is the refractive anisotropy of the **liquid crystal** molecule.

An INDEPENDENT CLAIM is also included for a method of making an in-plane switching mode (**LCD**) device having first and second substrates comprising:

(a) forming gate and data bus lines defining pixel regions and arranged on the first substrate;

(b) forming a common line in the pixel regions;

(c) forming a pair of first and second electrodes parallel to each other, applying plane electric fields in the pixel regions; and

(d) forming a **liquid crystal** layer between the first and second substrates.

USE - None given.

ADVANTAGE - The in-plane switching mode **liquid crystal** display (**LCD**) device has high light transmittance by controlling the refractive anisotropy of the **liquid crystal** molecule and the thickness of the **liquid crystal** layer. The **LCD** prevents color-shift.

Dwg.0/3

L71 ANSWER 17 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1999-575139 [49] WPIX
DNN N1999-424298 DNC C1999-167888
TI Active **matrix liquid crystal** substrate for thin film transistor - has layer insulation film consisting of baking products having per hydro poly silazane.
DC L03 P81 U12 U14
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 11249168 A 19990917 (199949)* 7p
ADT JP 11249168 A JP 1998-52456 19980304
PRAI JP 1998-52456 19980304
AB JP 11249168 A UPAB: 19991124

NOVELTY - The layer insulation film of thin film transistor consists of baking products having per hydro poly silazane. The per hydro poly silazane includes **silicon oxide**, **silicon nitride** and hydroxylation silicon.

An INDEPENDENT CLAIMs are also included for manufacturing method of active **matrix** substrate.

USE - For thin film transistor used in **liquid crystal** display device.

ADVANTAGE - Offer flattened TFTs resulting in flat **pixel electrode** formation. Improves screen brightness. Offers array formation of **pixel electrode** on substrate at the shape of **matrix**. Improves performance of **liquid crystal** panel.

DESCRIPTION OF DRAWING(S) - The figure shows partial cross- sectional view of **liquid crystal** panel of active **matrix** substrate.

Dwg.1/4

L71 ANSWER 18 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1999-504556 [42] WPIX

DNN N1999-377364 DNC C1999-147863
TI TFT production for active **matrix** type **LCD** panel for view finder and projector of PDA - comprises removing resist film by ashing, after ion implantation into silicon film of n-channel TFT formation area.
DC L03 P81 P85 U12 U14
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 11220134 A 19990810 (199942)* 8p
ADT JP 11220134 A JP 1998-21959 19980203
PRAI JP 1998-21959 19980203
AB JP 11220134 A UPAB: 19991014
NOVELTY - A protective film (15) comprising **silicon nitride** or **silica** is formed on a silicon film (12). A resist film (16) is formed on the protective film of a p-channel TFT formation area (A). Ion implantation is performed into the silicon film of the n-channel TFT formation area (3). The resist film is then removed by ashing.
USE - For an active **matrix** type **LCD** panel used for the view- finder and projector of PDAs or video cameras.
ADVANTAGE - Since the silicon film is **etched** during ashing of the resist film, damage to the silicon film or gate insulating film is prevented. Resist scum remaining after ashing is removed, avoiding defect generation. Improves yield and manufactures TFT with favourable characteristic.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of semiconductor manufacture. (3) TFT formation area; (12) Si film; (15) Protective film; (16) Resist film.
Dwg.2/15

L71 ANSWER 19 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1999-253975 [21] WPIX
CR 1997-131808 [12]
DNN N1999-189058
TI Thin film transistor (TFT) for **liquid crystal** display (**LCD**).
DC U12 U14
IN CHEN, L; TSAI, H
PA (INTE-N) IND TECHNOLOGY RES INST
CYC 1
PI US 5892246 A 19990406 (199921)* 8p
ADT US 5892246 A Div ex US 1996-663441 19960613, Cont of US 1996-762484 19961209, US 1997-974020 19971119
FDT US 5892246 A Div ex US 5602047
PRAI US 1996-663441 19960613; US 1996-762484 19961209; US 1997-974020 19971119
AB US 5892246 A UPAB: 19990603
NOVELTY - A **gate electrode** (72) of width 10-30 microns, is formed on borosilicate glass substrate (71). An amorphous silicon layer (74) is heavily doped on the area other than gate formation area. Metallic **source** and **drain electrodes** (83) are formed on heavily doped amorphous polysilicon layer and **silicon nitride** or **silicon oxide** layer (82) is formed on entire surface.
DETAILED DESCRIPTION - The radiation range of borosilicate is from 350-25,000 Angstrom. Gate material is selected from one amount tantalum, chromium, molybdenum or aluminum with thickness of 2000-4000 Angstrom. An insulating dielectric layer is one among **silicon oxide**, **silicon nitride**, tantalum oxide of thickness 2000-4000 Angstrom. The metallic layer is selected from one among aluminum, titanium or molybdenum.

USE - For active **matrix liquid crystal** display.

ADVANTAGE - Since a parasitic capacitance between gate and source is decreased, TFT structure is well suited for production of large panel active **matrix LCD**.

DESCRIPTION OF DRAWING(S) - The figure shows the structure of TFT.

Borosilicate glass 71

Gate electrode 72

Insulating layer 73

Amorphous silicon layer 74

Silicon nitride (or) **silicon oxide** layer 82

Source and **drain electrodes** 83

Dwg.11/12

L71 ANSWER 20 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1999-189787 [16] WPIX
DNN N1999-138818 DNC C1999-055799
TI Nano scale illumination device using gas discharge.
DC L03 S02 T01 T04 U14 W01 W05 X22 X26
IN MORGAN, C O; RUTTEN, M J; WALTON, E G; WRIGHT, T M
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5877589 A 19990302 (199916)* 5p
ADT US 5877589 A US 1997-819346 19970318
PRAI US 1997-819346 19970318
AB US 5877589 A UPAB: 19990424

NOVELTY - The device has a **matrix** material (10), with nanometer sized sealed cavities (12) containing ionizable noble gases, thus producing different colors from the different gases when ionized by an electrical field from electrodes (18, 20).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the production of the device. An ionizable gas is captured within the cavities formed in the **matrix**. The **matrix** is then oriented within the field region from a field generator (18, 20).

Preferred Features: The gas is neon, argon, krypton or xenon. The **matrix** material is **silicon dioxide**, aluminum oxide, **silicon nitride**, polymer or other insulator. The gas may be captured by: (a) forming **openings** in the **matrix**, and coating the **openings** with a sealant in an atmosphere containing the gas; (b) bubbling the gas through the **matrix** material whilst it is viscous, and then solidifying; or (c) mixing the **matrix** while viscous with a solid precursor of the gas, solidifying, and then converting the precursor.

USE - Backlighting plates for displays such as **LCD** screens in personal computers, pagers, phones, etc.; or as stand alone low level lighting sources for gauges, vehicle dashboards and instrument panels.

ADVANTAGE - Since the cavities can be filled with various different gases, the range of colors is increased.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional side view of the device.

matrix (10)

sealed cavities (12)

observer (14)

optical fiber or photo multiplier tube (16)

electrodes (18, 20)

dielectric substrate (22)

Dwg.1/3

L71 ANSWER 21 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1998-221140 [20] WPIX

DNN N1998-174997
TI Reflection and projection **LCD** device - has taper stand which performs taper processing of edge of thin **silicon oxide** or **silicon nitride** film.
DC P81 U14
PA (HITA) HITACHI LTD
CYC 1
PI JP 10062797 A 19980306 (199820)* 5p
ADT JP 10062797 A JP 1996-217067 19960819
PRAI JP 1996-217067 19960819
AB JP 10062797 A UPAB: 19980528
The device includes an active **matrix** substrate (4) consisting of an active element (1), a **pixel electrode** (2) and a semiconductor substrate (3). An opposing substrate (7) that consists of a transparent electrode (5) and a glass substrate (6) is provided opposing the active **matrix** substrate.

A **liquid crystal** (8) is supported between the active **matrix** substrate and the opposing substrate. A thin **silicon oxide** film or **silicon nitride** film is formed on the bottom of **pixel electrode** edge. A taper stand (16) performs taper processing of the edge of thin film.

ADVANTAGE - Reduces horizontal electric field between adjacent pixels. Improves contrast characteristics of **LCD** device.
Dwg.1/6

L71 ANSWER 22 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1998-185671 [17] WPIX
CR 1992-286104 [35]; 1993-186082 [23]; 1993-381162 [48]; 1994-010822 [02]; 1994-010823 [02]; 1994-016802 [03]; 1994-038407 [05]; 1994-068409 [09]; 1994-069941 [09]; 1994-228666 [28]; 1994-297831 [37]; 1994-352611 [44]; 1994-352612 [44]; 1996-458685 [46]; 1999-067035 [06]; 1999-112307 [10]; 1999-127636 [11]; 1999-410731 [35]; 2000-132661 [12]; 2000-187992 [17]; 2000-275998 [24]; 2001-215164 [22]; 2002-323093 [36]; 2002-422617 [45]
DNN N1998-147514
TI Insulated gate FET for active **matrix liquid crystal** device - has gate insulating layer which includes **silicon oxide** film formed on semiconductor layer containing source, drain and channel areas.
DC P81 U11 U12 U14
PA (SEME) SEMICONDUCTOR ENERGY LAB
CYC 1
PI JP 10041520 A 19980213 (199817)* 19p
ADT JP 10041520 A Div ex JP 1992-187604 19920622, JP 1997-102689 19920622
PRAI JP 1992-187604 19920622; JP 1997-102689 19920622
AB JP 10041520 A UPAB: 20021129
The device has an insulated substrate (105) on the surface of which a semiconductor layer is formed. The semiconductor layer contains a source area (100), a drain area (101) and a channel area (109). A gate insulating layer (110) which includes **silicon oxide** film is formed on the semiconductor layer. A **gate electrode** (111) is formed on the gate insulating layer. An anodised film is coated on the surface of the **gate electrode**. A **source electrode** (102) and a **drain electrode** (103) are connected to the respective source and drain areas.

An interlayer insulating film is formed between the **source** and **drain electrodes**. First and second signal lines are extended from the gate and **drain electrodes**, respectively. The interlayer insulating film consists of **silicon nitride** or aluminium oxide.

ADVANTAGE - Reduces leak current during reverse bias. Obtains favourable display quality. Improves yield of device.

Dwg.1/21

L71 ANSWER 23 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1998-055988 [06] WPIX
DNN N1998-044419 DNC C1998-019258
TI Manufacturing thin film transistor for **liquid crystal** display - involves surface treating semiconductor layer and forming second insulating layer using organic material to prevent creation of charge traps.
DC A85 E19 L03 P81 P85 U11 U12 U14
IN KIM, J H; PARK, S I; PARK, S
PA (GLDS) LG ELECTRONICS INC; (GLDS) LG PHILIPS LCD CO LTD; (GLDS) KINSEISHA KK
CYC 6

PI	GB 2315158	A	19980121 (199806)*	34p
	DE 19729176	A1	19980122 (199809)	20p
	FR 2751131	A1	19980116 (199810)	27p
	JP 10082997	A	19980331 (199823)	11p
	GB 2315158	B	19990210 (199909)	
	KR 98010547	A	19980430 (199915)	
	KR 98010548	A	19980430 (199915)	
	KR 213966	B1	19990802 (200104)	
	KR 213967	B1	19990802 (200104)	
	US 6188452	B1	20010213 (200111)	
	DE 19729176	C2	20020425 (200230)	

ADT GB 2315158 A GB 1997-14111 19970703; DE 19729176 A1 DE 1997-19729176 19970708; FR 2751131 A1 FR 1997-8020 19970626; JP 10082997 A JP 1997-191987 19970702; GB 2315158 B GB 1997-14111 19970703; KR 98010547 A KR 1996-27653 19960709; KR 98010548 A KR 1996-27655 19960709; KR 213966 B1 KR 1996-27655 19960709; KR 213967 B1 KR 1996-27653 19960709; US 6188452 B1 CIP of US 1997-826804 19970325, US 1997-889096 19970707; DE 19729176 C2 DE 1997-19729176 19970708
FDT US 6188452 B1 CIP of US 6100954
PRAI KR 1996-27655 19960709; KR 1996-27653 19960709
AB GB 2315158 A UPAB: 19980209
Manufacture of a thin film transistor for an active **matrix** **liquid crystal** display involves (i) surface treating the semiconductor layer (122), and (ii) forming a second insulation layer (123) on the semiconductor layer using organic material. The transistor includes a **gate electrode** branched off from a gate line, the semiconductor layer, an ohmic **contact** layer, a source and a **drain electrode** branched off from a data bus line, and the second insulation layer.

Also claimed are (a) the **LCD** including the thin film transistor, and (b) a semiconductor switching element and its manufacture involving plasma treatment of the semiconductor layer and/or the organic insulating layer.

USE - The TFT functions as a switching element for the **LCD**.

ADVANTAGE - The plasma treatment forms a stable bond structure of **Si-O** or **Si-N** on the surface. The interfacial problems between the semiconductor and the organic insulation layers such as charge trap and detachment can be eliminated.
Dwg.16H/17

L71 ANSWER 24 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1997-361295 [33] WPIX
DNN N1997-300352
TI Thin film transistor array used in active **matrix** type **LCD** element - in which **silicon nitride** film of interlayer insulating film has high dielectric constant compared to that

of **silicon oxide** film.
DC P81 U11 U12 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 09153617 A 19970610 (199733)* 5p
ADT JP 09153617 A JP 1995-311237 19951129
PRAI JP 1995-311237 19951129
AB JP 09153617 A UPAB: 19970820
The array has an insulating substrate (1) on which an auxiliary capacitive electrode (2) is formed selectively using an electrically conductive material. An interlayer insulating film made of two layers is formed which covers the capacitive electrode and substrate. The first layer comprises a **silicon nitride** film (3) and the second layer comprises a **silicon oxide** film (4). A **drain electrode** (6) and a display electrode (5) are formed selectively on the **silicon oxide** film.

A non-crystal silicon film (7) is formed on the **silicon oxide** film, such that it overlaps on the **drain** and display **electrodes**. A gate insulating film (8) and a **gate electrode** (9) are layered orderly on the non-crystal silicon film. The **silicon nitride** film of the interlayer insulating film has a high dielectric constant compared to that of the **silicon oxide** film.

ADVANTAGE - Enlarges storage capacitive of auxiliary capacitive electrode. Prevents short circuit between electrodes. Improves transistor characteristics.
Dwg.1/4

L71 ANSWER 25 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1997-124941 [12] WPIX
DNN N1997-103191 DNC C1997-040104
TI Semiconductor IC mfg method for e.g. dual gate type TFT used as switching element in active **matrix LCD** device - involves forming source-drain areas on either side of active layer area and also on acid **SiN** film.
DC L03 U11 U12 U14
PA (CITL) CITIZEN WATCH CO LTD
CYC 1
PI JP 09008309 A 19970110 (199712)* 19p
ADT JP 09008309 A JP 1995-147953 19950615
PRAI JP 1995-147953 19950615
AB JP 09008309 A UPAB: 19970320
The mfg method involves forming a **silicon oxide** film (13) on the selected portion of a Si substrate (11). An acid **SiN** film (15) is formed on the **silicon oxide** film. A lower **gate electrode** (17) containing a polycrystalline silicon film is formed on the selected portion of the **SiN** film. A lower gate insulating film (29) covers the peripheral surface of the **gate electrode**.

An active layer area (23) is formed on the portion of the lower gate insulating film. A source-drain areas (25,27) are formed on either side of the active layer area and also on the **SiN** film. An upper gate insulating film (31) i.e polycrystalline silicon film is formed on the active layer area including source-drain areas suitably. A **gate electrode** (19) is formed on the portion of the gate insulating film, corresponding to the active layer area.

USE/ADVANTAGE - For three dimensional circuit element. Improves insulation destruction breakdown voltage. Improves control of threshold voltage value.
Dwg.8/13

L71 ANSWER 26 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1997-068863 [07] WPIX
DNN N1997-056665
TI TFT array substrate used in **liquid crystal** HD display device - in which drain wiring of **drain electrode** of TFT, transparent electrically conductive film and second metal layer are formed in stacked fashion.
DC P81 U12 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 08313934 A 19961129 (199707)* 10p
ADT JP 08313934 A JP 1995-122452 19950522
PRAI JP 1995-122452 19950522
AB JP 08313934 A UPAB: 19970212
The substrate comprises a **gate electrode** (2) installed on the principal plane of a glass substrate (1). A first gate insulating film (8) composed of **silicon oxide** is layered over the substrate. An intrinsic type amorphous silicon layer (6) of high resistance is deposited over the insulating film, corresponding to the formation zone of the **gate electrode**. A pair of N type polycrystalline silicon layer (7,8) of low resistance is formed adjacent to the amorphous silicon layer. A transparent electrically conductive film (17) and an ITO molybdenum layer (12) are layered over it thereby forming a **source electrode** (13) and a **drain electrode** (14). The electrodes are mounted over the low resistance layers.

A display **pixel electrode** (15) is installed on the gate insulating film is connected to the **source electrode**. Then, a protection insulating film (18) composed of **silicon nitride** is formed over a TFT (17). Thus, a TFT **matrix** bearing substrate (19) is constituted. Stacked arrangement of a colour filter (22) and a countering electrode (23) is provided over the glass substrate. A **liquid crystal** (29) is positioned between the substrate and an opposite substrate (24). Drain wiring part corresponding to the **drain electrode** of TFT is then formed.

ADVANTAGE - Prevents reduction in yield and reduction in performance. Simplifies setting up of **etching** ratio. Simplifies mfg process. Curtails number of mfg processes.
Dwg.1/26

L71 ANSWER 27 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1996-271055 [28] WPIX
DNN N1996-227797
TI Thin film transistor for active **matrix** type **LCD** circuit - has **silicon oxide** layer set up between protection layer and amorphous silicon layer exposing top portion of electrode alone.
DC U12
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 07221309 A 19950818 (199628)* 4p
ADT JP 07221309 A JP 1994-9959 19940131
PRAI JP 1994-9959 19940131
AB JP 07221309 A UPAB: 19960719
The transistor has an insulating glass substrate (1) along with a **gate electrode** (2) covered with a gate insulation layer (3). A **silicon oxide** layer (12) is placed in between **silicon nitride** and amorphous silicon layers to form a channel area (4) covered by a protection layer (13).

In addition to the protection layer, two or more high insulated

silicon oxide layers are provided to cover the entire channel area.

ADVANTAGE - Realises good performance and switching characteristics with lesser power consumption.

Dwg.1/3

L71 ANSWER 28 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1996-144777 [15] WPIX
DNN N1996-121545 DNC C1996-045422
TI Thin film transistor for active **matrix** type **LCD** device - has source drain domain which is formed on either sides of channel domain made of polycrystalline silicon.
DC L03 U12
PA (SONY) SONY CORP
CYC 1
PI JP 08032083 A 19960202 (199615)* 6p
ADT JP 08032083 A JP 1994-186743 19940715
PRAI JP 1994-186743 19940715
AB JP 08032083 A UPAB: 19960417

The TFT (1) consists of a metal **gate electrode** (12) which is formed on the surface of a glass substrate (11). A metal oxide film (13) is formed on the metal oxide electrode by performing anodic oxidation. A gate insulation film (14) comprising a **silicon nitride** film (21) and a **silicon oxide** film (22) is also formed on the metal oxide film.

A channel domain (15) which consists of a polycrystalline silicon is then formed on the upper surface of the gate insulation film. A pair of source drain domains (17,18) are formed on either sides of the channel domain.

ADVANTAGE - Raises electron mobility. Improves transistor characteristics. Improves reliability of TFT.

Dwg.1/5

L71 ANSWER 29 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1996-066726 [07] WPIX
CR 2002-118261 [16]; 2002-309836 [35]
DNC C1996-021777
TI Semiconductor device with TFT for active **matrix** type **LCD** device - has passivation film with **silicon nitride** as main ingredient which is coated on whole surface of device.
DC L03 U11 U14
IN UOCHI, H
PA (SEME) SEMICONDUCTOR ENERGY LAB
CYC 2
PI JP 07326766 A 19951212 (199607)* 8p
US 5897345 A 19990427 (199924)
US 6133620 A 20001017 (200054)#
US 6462403 B1 20021008 (200269)
ADT JP 07326766 A JP 1994-142448 19940531; US 5897345 A Cont of US 1995-451649 19950526, US 1997-803865 19970221; US 6133620 A Cont of US 1995-451649 19950526, Div ex US 1997-803865 19970221, US 1998-222730 19981229; US 6462403 B1 Cont of US 1995-451649 19950526, Div ex US 1997-803865 19970221, Div ex US 1998-222730 19981229, US 2000-641769 20000821
FDT US 6133620 A Div ex US 5897345; US 6462403 B1 Div ex US 5897345, Div ex US 6133620
PRAI JP 1994-142448 19940531; US 1998-222730 19981229
AB JP 07326766 A UPAB: 20021026

The semiconductor device has an aluminium film (108) which is formed over the whole surface of a **silicon oxide** film (107). An anode oxide film (109) is formed over the surface of the aluminium film by anodic oxidation process. The anodic oxidation process is carried out by

passing current through an electrolytic solution.
Etching of the aluminium film and the anode oxide film is then performed to form an aluminium wiring (110). The surface of the aluminium wiring gets hidden under the anode oxide film. A passivation film (111) with **silicon nitride** as the main ingredient is then coated over the surface of the device.
ADVANTAGE - Prevents hillock generation in aluminium wiring since passivation film is formed over its surface. Reduces poor location of short wiring. Increases rate of excellent article of IC.
Dwg.1/4

L71 ANSWER 30 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1996-022351 [03] WPIX
DNN N1996-018567
TI Black **matrix liquid crystal** screen mfr. method with storage capacity - by forming planar conductor with transparent equipotential first layer and **etched** opaque layer which is partly oxidised.
DC P81 U14
IN KROEBER, W; SZYDLO, N; VIGNOLLE, J
PA (CSFC) THOMSON-LCD
CYC 1
PI FR 2720170 A1 19951124 (199603)* 11p
ADT FR 2720170 A1 FR 1994-5986 19940517
PRAI FR 1994-5986 19940517
AB FR 2720170 A UPAB: 19960122
The method involves a transparent layer (2) made of indium tin oxide on an insulating transparent substrate (1). An opaque layer (3) is then formed by oxygen plasma or by anodic oxidation of tantalum. A resinous deposit masks parts of the opaque layer during photoetching to form the passive dark regions.
An insulating layer (6) is formed on the black **matrix** by anodic oxidation of the opaque layer. A dielectric layer (4) e.g. **silicon dioxide** or **silicon nitride** is formed over the previous layers to support the active thin layers of the screen.
ADVANTAGE - Avoids short-circuits which reduces picture quality without increasing complexity.
Dwg.1d/1

L71 ANSWER 31 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1995-033555 [05] WPIX
CR 1989-196030 [27]
DNN N1995-026676 DNC C1995-015314
TI Thin film transistors for active **matrix** type **LCD** - uses gate insulating film consisting of **silicon oxide** film and silicon nitriding film where thickness of **silicon oxide** film is greater than thickness of silicon nitriding film.
DC L03 U12 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 06318704 A 19941115 (199505)* 5p
ADT JP 06318704 A Div ex JP 1987-290520 19871119, JP 1993-329614 19871119
PRAI JP 1987-290520 19871119; JP 1993-329614 19871119
AB JP 06318704 A UPAB: 19950207
The TFT has a **gate electrode** (2) on a substrate (1). At the sides of **gate electrode** and on the **gate electrode**, a gate insulating film (3) is formed. The gate insulating film consists of two layers viz a **silicon oxide** film (3a) and a **silicon nitride** film (3b). The thickness of the **silicon oxide** film is

greater than that of the **silicon nitride** film. The thickness of the **silicon oxide** film is greater than 0.3 microns, and the thickness of the **silicon nitride** film varies from 0.025 to 0.125 microns.

ADVANTAGE - Provides high reliability.

Dwg.1/5

L71 ANSWER 32 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1994-288153 [36] WPIX
DNN N1994-226909 DNC C1994-131314
TI Active **matrix** type **LCD** device - has silicon film formed on protection film comprising **silicon oxide** or nitride, on picture element electrode.
DC L03 P81 U14
PA (HITA) HITACHI LTD
CYC 1
PI JP 06214253 A 19940805 (199436)* 14p
ADT JP 06214253 A JP 1993-4723 19930114
PRAI JP 1993-4723 19930114
AB JP 06214253 A UPAB: 19941102
A Si film is formed on a protection film having a **hole** and comprising a **silicon oxide** film or a **silicon nitride** film on a transparent picture element electrode.

ADVANTAGE - Deterioration of display characteristic and an increase of OFF current may be prevented.

Dwg.15/15

L71 ANSWER 33 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1994-257700 [32] WPIX
DNN N1994-203135 DNC C1994-117798
TI **Liquid crystal** display device - includes **pixel electrode** formed through layer insulation film and drive circuit inside seal part.
DC A85 L03 P81 P85 T04 U14
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 06186578 A 19940708 (199432)* 3p
ADT JP 06186578 A JP 1992-337489 19921217
PRAI JP 1992-337489 19921217
AB JP 06186578 A UPAB: 19940928
The **liquid crystal** display device of active **matrix** system consists of a glass substrate (101) a pixel (102) and a **pixel electrode** (106). These are assembled through layer insulation films such as polyimide resin, **silicon dioxide** film and **silicon nitride** film. A thin film transistor drive (103) is positioned inside a seal part (110). The pixel display area (108) is at the centre.

There is no conductive film on the drive circuit and an opposite electrode (111) formed on a substrate (107) overlaps with the pixel part and drive circuit. The upper and lower substrates are linked by a adhesive agent (109).

ADVANTAGE - Allows miniaturisation of device. Improves moisture resistance. Increases device reliability. Minimises influence of external electric field.

Dwg.1/3

L71 ANSWER 34 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1993-288596 [36] WPIX
DNN N1993-221937
TI Addressable **matrix** display applying electric field to electro-optical material - has one electrode of transparent doped

semiconductor forming channel of control transistor whose drain or source is provided by electrode.

DC P81 P85 U14 V07
IN LEHUREAU, J; MAGARINO, J
PA (CSFC) THOMSON-LCD
CYC 18
PI WO 9317364 A1 19930902 (199336)* FR 20p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: JP US
FR 2687824 A1 19930827 (199345)
ADT WO 9317364 A1 WO 1993-FR168 19930219; FR 2687824 A1 FR 1992-1999 19920221
PRAI FR 1992-1999 19920221
AB WO 9317364 A UPAB: 19931122
Two electrodes are situated at each pixel to display the image. The transparent electrode (15) is surrounded by an amorphous region (17) comprising silicon deposited in hydrogen-free conditions. One part (18) of the amorphous region forms a channel which may be lightly doped or undoped; this may be achieved by crystallising the silicon using an argon laser.

The underlying layers are built up by LPCVD on a glass base (10) and are successively **silica** (11), insulation (13) such as **silicon nitride** and metal (14), which are subsequently **etched** to form a grid. The electro-optical material is placed between a substrate that comprises the transparent electrode columns and a substrate that includes the transparent semiconducting lines.

USE/ADVANTAGE - **Liquid crystal** display. Reduces currents in blocked state and fixed noise on screen.
Dwg.5/6

L71 ANSWER 35 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1992-068810 [09] WPIX
DNN N1992-051586 DNC C1992-031409
TI Active **matrix** type **liquid crystal** display - with surface protection films of **silicon oxide**, silicon oxynitride and **silicon nitride** on semiconductor in **etched** channel.
DC L03 P81 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 04012330 A 19920116 (199209)*
ADT JP 04012330 A JP 1990-112639 19900430
PRAI JP 1990-112639 19900430
AB JP 04012330 A UPAB: 19931006
Active **matrix** type **liquid crystal** display has a surface protective film formed on a back channel formed by **etching**. The surface protective film consists of a **silicon oxide** film formed in **contact** with the semiconductor silicon on the back channel, a silicon oxynitride film formed on the **silicon oxide** film, and a **silicon nitride** film formed on the silicon oxynitride film. The compsn. of the silicon oxynitride film changes gradually from the **silicon oxide** film side to the **silicon nitride** film side.

USE/ADVANTAGE - Active **matrix** type **liquid crystal** display formed of thin film transistor (TFT), etc. Occurrence of cracks and film separation can be avoided, and, further, the barrier effect against alkali ions is high. Thus, production yield is high, and the initial characteristics are better than those of the conventional ones.
3/4

L71 ANSWER 36 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1988-004210 [01] WPIX
DNN N1988-002989 DNC C1988-002017
TI Active **matrix** wafer using thin-film transistor - has increased reliability due to use of specific protective layer contg. tantalum aluminium and oxygen.
DC L03 P81 P85 U14
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 62269120 A 19871121 (198801)* 3p
PRAI JP 1986-113087 19860516
AB JP 62269120 A UPAB: 19930923
In an active **matrix** wafer using a thin-film transistor the first conductor layer is formed selectively on an insulator base plate by partly overlapping it on a non-crystal Si semiconductor through an insulator layer of **silicon nitride** or **silicon oxide**. A source and a **drain electrode** of Al, etc., are formed by partly overlapping them on the non-crystal Si semiconductor layer, a protective layer of TaxAlyO5 or BaTa2O6, having a thickness of about 5000 Angstroms, is formed on the **source electrode** and the **drain electrode** by RF sputtering, etc.
USE/ADVANTAGE - The active **matrix** wafer to be used in **liq. crystal** displays, etc.,can greatly raise the reliability of the **liq. crystal** display because of the use of the specific protective layer, as compared with ones using the conventional protective layer of **silicon nitride** or **silicon oxide**.
3/6

L71 ANSWER 37 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1987-051576 [08] WPIX
DNN N1987-039108 DNC C1987-021462
TI FET **gate electrode** prodn. - involving plasma ashing of resist used in electrode patterning.
DC G06 L03 P81 P85 U11 U14
IN PARKS, H G; POSSIN, G E; POSSIN, G
PA (GENE) GENERAL ELECTRIC CO
CYC 6
PI EP 211370 A 19870225 (198708)* EN 12p
R: FR GB SE
FR 2585879 A 19870206 (198711)
US 4646424 A 19870303 (198711) 11p
JP 62072167 A 19870402 (198719)
DE 3636220 A 19880428 (198818)
EP 211370 B 19911016 (199142)
R: FR GB SE
JP 2637078 B2 19970806 (199736) 9p
DE 3636220 C2 19990211 (199910)#
ADT EP 211370 A EP 1986-110376 19860728; FR 2585879 A FR 1986-11188 19860801; US 4646424 A US 1985-761937 19850802; JP 62072167 A JP 1986-180273 19860801; DE 3636220 A DE 1986-3636220 19861024; JP 2637078 B2 JP 1986-180273 19860801; DE 3636220 C2 DE 1986-3636220 19861024
FDT JP 2637078 B2 Previous Publ. JP 62072167
PRAI US 1985-761937 19850802
AB EP 211370 A UPAB: 19930922
Gate electrode material is deposited in an inverted thin film FET by (i) forming a titanium layer on an insulating substrate, pref. pre-coated with a **silicon oxide** layer; (ii) coating the titanium layer with positive photoresist; (iii) exposing the photoresist through a mask to form a desired pattern of exposed resist;

(iv) developing the resist layer; (v) plasma **etching** the titanium beneath the exposed resist; (vi) plasma ashing the remaining resist in an oxygen atmos.; and (vii) stripping the remaining resist.

USE/ADVANTAGE - The process is esp. useful in mfr. of FETs for **matrix** addressed **LCDs** and allows reliable and high yield mfr. of responsive high resolution **LCDs** by process compatible with conventional VLSI techniques. A hardened gate material, which is more immune to **etchant** attack in subsequent processing, is formed and a protective **silicon nitride** layer is not required. The problem of undercutting is mitigated.

0/4

L71 ANSWER 38 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1986-306829 [47] WPIX
DNN N1986-229231
TI **Liquid crystal** display device e.g. for measuring instrument - has non-linear resistance elements including amorphous material formed on device substrate and connected in series with each other.
DC P81 P85 U14
IN SUZUKI, M
PA (DASE) SEIKO INSTR INC; (DASE) SEIKO INSTRUM ELTRN
CYC 10
PI EP 202092 A 19861120 (198647)* EN 14p
R: CH DE FR GB IT LI SE
JP 61260219 A 19861118 (198706)
CA 1258547 A 19890815 (198941)
US 4871234 A 19891003 (198949)
EP 202092 B1 19920812 (199233) EN 14p
R: CH DE FR GB IT LI SE
DE 3686351 G 19920917 (199239)
ADT EP 202092 A EP 1986-303579 19860512; JP 61260219 A JP 1985-103141 19850515; US 4871234 A US 1989-325100 19890314; EP 202092 B1 EP 1986-303579 19860512; DE 3686351 G DE 1986-3686351 19860512, EP 1986-303579 19860512
FDT DE 3686351 G Based on EP 202092
PRAI JP 1985-103141 19850515
AB EP 202092 A UPAB: 19930922
Each non-linear resistance element includes a conductor formed by a row electrode (4) or a column electrode (7), a second conductor formed by the other one of the row or column electrode and a **pixel electrode** (2). The amorphous material (3) formed between the two conductors consists mainly of silicon. Pref. the amorphous material is **silicon dioxide**, **silicon nitride** or **silicon oxide** nitride with a silicon content in excess of the stoichiometric ratio.

The material is formed as a film of thickness between four hundred Angstroms and one micron. Hydrogen phosphorous or boron may be included in the material.

USE/ADVANTAGE - Display panel of measuring instrument, motor vehicle instrument panel personal computer image display or television receiver. Symmetrical voltage-current characteristics are achieved relative to polarity of voltage applied to electrodes. Non-linear resistance elements have sufficient breakdown strength not to be destroyed by static electricity.

1b/11

L71 ANSWER 39 OF 63 WPIX (C) 2003 THOMSON DERWENT
AN 1982-B0425E [05] WPIX
TI **Liq. crystal** information display - uses planar transistor array with transparent layer providing different colour

displays according to chemical composition.
DC P81 P85 U14 W05
IN HATANAKA, K; NAKAGIRI, T; OKUBO, Y; OSADA, Y; SUGATA, M
PA (CANO) CANON KK
CYC 3
PI DE 3113041 A 19820128 (198205)* 102p
JP 59046628 A 19840316 (198417)
US 4470667 A 19840911 (198439)
JP 60068326 A 19850418 (198522)
US 4761058 A 19880802 (198833)
DE 3153620 A 19890824 (198935)
DE 3113041 C 19900628 (199026)
DE 3153620 C 19920123 (199204)
US 35275 E 19960618 (199630) 30p
US 36161 E 19990323 (199919)
ADT JP 59046628 A JP 1983-122007 ; US 4470667 A US 1983-547443 19831031; JP 60068326 A JP 1984-148309 19800507; US 4761058 A US 1985-814277 19851223; US 35275 E Cont of US 1981-246161 19810323, Div ex US 1983-547443 19831031, Cont of US 1984-632024 19840718, US 1985-814277 19851223, Cont of US 1990-562108 19900802, Cont of US 1992-823605 19920117, Cont of US 1993-15898 19930210, Cont of US 1993-153488 19931117, US 1995-464368 19950605; US 36161 E Cont of US 1981-246161 19810323, US 1983-547443 19831031, Cont of US 1995-421515 19950413, US 1997-888791 19970707
FDT US 35275 E Div ex US 4470667, Reissue of US 4761058; US 36161 E Reissue of US 4470667
PRAI JP 1980-43101 19800401; JP 1980-44461 19800402; JP 1980-45941 19800408; JP 1980-66238 19800519; JP 1984-148309 19800507
AB DE 3113041 A UPAB: 19930915
The appts. has a hinged, metal, reflective, lid which fits over the display area. The planar transistors are between one electrode with a metal reflective surface and a further transparent electrode which generate electro-optical images by controlling the incident eight. The display may be a **liquid crystal** arrangement in a number of colours e.g. purple, blue, yellow, magenta-green, orange and cyan.

Thin film planar transistors may be used which are provided with isolation layers on their light emitting regions. This layer may be formed from silicon monoxide **silicon dioxide**, aluminium oxide, titanium oxide, magnesium fluoride, calcium fluoride, or **silicon nitride**.
1,2

L71 ANSWER 40 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 2002-196699 JAPIO
TI ACTIVE **MATRIX** SUBSTRATE AND **LIQUID CRYSTAL** DISPLAY DEVICE
IN NONAKA MASANOBU; YONEKURA TOSHIMASA
PA TOSHIBA CORP
PI JP 2002196699 A 20020712 Heisei
AI JP 2000-393369 (JP2000393369 Heisei) 20001225
PRAI JP 2000-393369 20001225
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide an active **matrix** substrate, in which a conductive film is prevented from being peeled or shaved off caused by stress at the time of packaging peripheral circuits. SOLUTION: The conductive film composing a power-feeding electrode to a signal line 11 and a scanning line is covered with an insulation protecting film 35 of **silicon nitride** or an interlayer insulating film 34 of **silicon oxide** and the insulation protecting film 35 of **silicon nitride**. A plurality of

contact holes 35a are formed in a power-feeding electrode area. An electrode film 36 to be connected with the conductive film through these **contact holes** is formed by lamination. Even if aluminum is employed for the conductive film, the aluminum of the conductive film can be prevented from being peeled or shaved off caused by the stress at the time of packaging the peripheral circuits.

L71 ANSWER 41 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1999-249171 JAPIO
TI ACTIVE **MATRIX** TYPE DISPLAY DEVICE AND MANUFACTURE THEREOF
IN OTANI HISASHI; OGATA YASUSHI
PA SEMICONDUCTOR ENERGY LAB CO LTD
PI JP 11249171 A 19990917 Heisei
AI JP 1998-62281 (JP10062281 Heisei) 19980226
PRAI JP 1998-62281 19980226
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a sufficient auxiliary capacitance and to raise an **opening** ratio by constituting the capacitance connected to a thin film transistor by a black mask, an inorganic layer in **contact** with the black mask and a picture element electrode in **contact** with the inorganic layer.
SOLUTION: The auxiliary capacitance 110 using the inorganic layer 105, the black mask 104 in **contact** with the inorganic layer 105 and the picture element electrode 109 in **contact** with the inorganic layer 105 is formed on an inter-layer insulation film composed of organic resin film. As the black mask 104, a valve metal or a metallic material provided with a light shielding property and electric conductivity is used. For instance, Al, Ta, Ti, Cr or TiN is used. Also, as the inorganic film 103, a dielectric constant is important and amorphous **silicon nitride** film, amorphous **silicon oxide** film, **silicon nitride**-oxide film (**SiO** <SB>x</SB>N<SB>y</SB>), DLC(diamond-like carbon) film, titan oxide or their laminated film is used. Also, as the picture element electrode 109, ITO which is electrically conductive film provided with the light shielding property is used and the **liquid crystal** display device of a transmission type is constituted.

L71 ANSWER 42 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1999-038394 JAPIO
TI **LIQUID CRYSTAL** DISPLAY DEVICE AND ITS PRODUCTION
IN NARUTAKI YOZO; NAGATA HISASHI; KUBO MASUMI; FUJIOKA KAZUYOSHI; SHIMADA NAOYUKI
PA SHARP CORP
PI JP 11038394 A 19990212 Heisei
AI JP 1997-193697 (JP09193697 Heisei) 19970718
PRAI JP 1997-193697 19970718
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To reduce the production cost and to make a display device light in weight, by providing a high molecular **liquid crystal** film where orientation control is performed as a **liquid crystal** layer on a base plate.
SOLUTION: A Cs wiring 5 is formed simultaneously with a **gate electrode** 12 on an insulating base plate 10 such as a glass base plate, and a gate insulating film 7 made of **silicon nitride** or **silicon oxide**, a semiconductor layer 15 made of amorphous silicon or polysilicon, and n<SP>+</SP> silicons 17 and 18 being an ohmic **contact** layer are successively formed. Then, the high molecular **liquid crystal** film,

where orientation control processing is previously performed, and, which is to be the **liquid crystal** layer 30, is formed on a picture element electrode 4 and a layer insulation film 8 on the base plate (active **matrix** side) 10 by using a laminating method. The side chain type high molecular **liquid crystal** obtained by combining polymer such as polymethacrylate, polyacrylate or polysiloxane as a principal chain and **liquid crystal** molecules as a side chain is used as the high molecular **liquid crystal** being the **liquid crystal** layer 30 because it must respond to electric field for itself.
COPYRIGHT: (C)1999,JPO

L71 ANSWER 43 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1998-253982 JAPIO
TI TRANSVERSE ELECTRIC FIELD SYSTEM ACTIVE **MATRIX** TYPE **LIQUID CRYSTAL** DISPLAY DEVICE
IN ANDO MASAHIKO; FUKAYA RITSUO; YAMAMOTO TSUNENORI; WAKAGI MASATOSHI
PA HITACHI LTD
PI JP 10253982 A 19980925 Heisei
AI JP 1997-59263 (JP09059263 Heisei) 19970313
PRAI JP 1997-59263 19970313
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To make it possible to avoid charge accumulation and to assure good image quality, by using holding capacitor parts having a reversible charge accumulation characteristic.
SOLUTION: The holding capacitor part 112 is formed as the structure obtd. by holding a first gate insulating layer 13 as an insulating layer for a capacitor consisting of a **silicon nitride** film with a **source electrode** 18 as a **source electrode** for the capacitor and a **gate electrode** 12 as a gate executed for the capacitor. If the holding capacitor part is constituted in such a manner, the barrier effect of a second gate insulating layer 14 consisting of a **silicon oxide** film disappears and, therefore, the electrons implanted into the **silicon nitride** film (the first gate insulating layer 13) return to the semiconductor layer 15 (including **drain electrode** 17 and **source electrode** 18) side when the threshold control voltage attains zero and the charge accumulation in the holding capacitor part 112 is averted. Accordingly, since the internal voltage occurring in the charge accumulation is no longer impressed on **liquid crystals**, the image defects, such as flicker and after-images, do not arise any more.
COPYRIGHT: (C)1998,JPO

L71 ANSWER 44 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1998-062797 JAPIO
TI **LIQUID CRYSTAL** DISPLAY DEVICE
IN OKUBO TATSUYA; HIROTA SHOICHI; ABE MAKOTO
PA HITACHI LTD
PI JP 10062797 A 19980306 Heisei
AI JP 1996-217067 (JP08217067 Heisei) 19960819
PRAI JP 1996-217067 19960819
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To improve a contrast by providing a **liquid crystal** display device with **pixel electrodes** for relieving the transverse electric fields between adjacent pixels.
SOLUTION: This **liquid crystal** display device comprises active elements 1, **pixel electrodes** 2, an active **matrix** substrate 4 consisting of a glass or semiconductor substrate 3, transparent electrodes 5, a counter substrate 7 consisting of a counter glass substrate 6, **liquid crystals** 8 held

between this active **matrix** substrate 4 and the counter substrate 7 and tapered bases 16. These tapered bases 16 are the **pixel electrode** ends between the adjacent pixels and are the thin films of **silicon oxide** or **silicon nitride** . If the taking angle of the projecting lens of the projection type **liquid crystal** display device of a reflection type of a normally white mode is defined as ϕ, the tapered bases 16 are worked within a range where the taper angle thereof is larger than ϕ/2 and smaller than (45°-ϕ/2).

L71 ANSWER 45 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1998-039334 JAPIO
TI ARRAY SUBSTRATE AND **LIQUID CRYSTAL** DISPLAY DEVICE
IN NAKAMURA KENJIRO; FUKUDA KAICHI
PA TOSHIBA CORP
PI JP 10039334 A 19980213 Heisei
AI JP 1996-195012 (JP08195012 Heisei) 19960724
PRAI JP 1996-195012 19960724
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To provide a **liquid crystal** display device with which the crack and peeling of **pixel electrodes** are prevented and the operation defect of the **pixel electrodes** by the influence of impurities and the influence of interference of light are prevented. SOLUTION: **Silicon nitride** films 15 are formed on thin-film transistors(TFTs) 14 and acrylic resin films 16 which are org. insulating films are formed thereon. **Contact holes** 17 are formed at the acrylic resin films 16 and silicon oxynitride films 18 are formed on the acrylic resin films 16 including the inner peripheral surfaces of the **contact holes** 17. The **pixel electrodes** 19 are electrically connected to the **drain electrodes** 5 of the TFTs 14 **via** the surfaces of the silicon oxynitride films 18 on the surfaces of the **contact holes** 17, by which an active **matrix** substrate 20 is formed. The conduction of the impurities, metal ions and water in the org. films is good and the operation defect of the **pixel electrodes** is affected with the **silicon oxide** films. The refractive indices between the polyimide resin films which are the org. insulating films and the **pixel electrodes** of ITO (indium tin oxide) vary too mush with the **silicon nitride** film that the interference of light occurs. These defects are prevented by the formation of the silicon oxynitride films.

L71 ANSWER 46 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1997-293877 JAPIO
TI WIRING STRUCTURE AND FORMATION THEREOF
IN MIYAGAWA MAKOTO
PA CASIO COMPUT CO LTD
PI JP 09293877 A 19971111 Heisei
AI JP 1996-129264 (JP08129264 Heisei) 19960426
PRAI JP 1996-129264 19960426
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To enable east and perfect removal of an anodic oxidation mask formed in the surface of a connection pad connected to a **gate electrode via** a gate line, after an anodic oxidation film is formed on the surface of the **gate electrode** for formation of a thin-film transistor in an active **matrix** type **liquid crystal** display unit. SOLUTION: Only the surface of a connection pad 14 is covered with an

anodic oxidation mask 17 made of **silicon oxide**, under which condition to pad is anodized to form an anodic oxidation film 18 on the surface of a **gate electrode** 12. Next, a gate insulating film 19 made of **silicon nitride** is formed all over the film 18. Thereafter, a **contact hole** 25 is made in the gate insulating film 19 and anodic oxidation mask 17 at their parts corresponding to a central part of the connection pad 19. In this case, the film 19 and mask 17 can be easily **etched** collectively. In addition, the mask 17 can be perfectly removed from on the top face of the pad 14 in the **contact hole** 25.

L71 ANSWER 47 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1997-252136 JAPIO
TI SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD, ACTIVE **MATRIX** ARRAY, AND **LIQUID CRYSTAL** DISPLAY
IN FURUTA MAMORU
PA MATSUSHITA ELECTRIC IND CO LTD
PI JP 09252136 A 19970922 Heisei
AI JP 1996-58918 (JP08058918 Heisei) 19960315
PRAI JP 1996-58918 19960315
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To improve a throughput in process, by reducing the time for doping impurities when a p-channel FET and an n-channel FET are formed on the same substrate.
SOLUTION: After a polycrystalline silicon thin film 13 is formed on a substrate 11, a gate insulating thin film 14 made up of a **silicon oxide** thin film 14a and a **silicon nitride** thin film 14b is formed. A **gate electrode** 15A of a p-channel FET is formed, and the **gate electrode** 15A on the n-channel FET side is covered with a **gate electrode** material 15. A boron ion is doped in the p-channel FET, and a **gate electrode** 15B is formed on the n-channel FET side. The **silicon nitride** thin film 14b as an upper film of the gate insulating film 14 is removed partly, and a phosphorous ion is doped. At this time, the phosphorous ion is doped through the double layer gate insulating film 14 into the p-channel FET, so the concentration of phosphorous can be reduced. Then, the quantity of implanted boron ion can be reduced as much as twice the phosphorous ion, and thereby the time for implanting the boron ion can be reduced.

L71 ANSWER 48 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1997-246558 JAPIO
TI THIN FILM TRANSISTOR, AND ACTIVE **MATRIX** ARRAY FOR **LIQUID CRYSTAL** DISPLAY, AND THOSE MANUFACTURE
IN FURUTA MAMORU; TSUTSU HIROSHI; KAWAMURA TETSUYA
PA MATSUSHITA ELECTRIC IND CO LTD
PI JP 09246558 A 19970919 Heisei
AI JP 1996-53553 (JP08053553 Heisei) 19960311
PRAI JP 1996-53553 19960311
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To materialize LDD structure without increasing the number of processes of doping, and reduce the OFF currents of a thin film transistor.
SOLUTION: A **silicon oxide** film 12 to serve as a buffer layer is made on a glass substrate 11, and thereon a polycrystalline silicon thin film 13 is made, and it is put in the shape of an active layer. On the film 13, a gate insulating film 14, using a **silicon oxide**, and a **gate electrode** 15, using Al-Zr alloy 10 atom % in Zr concentration, are made. A **silicon**

nitride film 16 is made to cover a part of the **gate electrode** 15 and a low concentration impurity implantation area of the film transistor, and then impurity implantation is performed, using phosphorous ions.

L71 ANSWER 49 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1997-092618 JAPIO
TI PRODUCTION OF POLYSILICON, THIN FILM TRANSISTOR AND FABRICATION THEREOF, AND **LIQUID CRYSTAL** DISPLAY
IN KAWAMURA SHINICHI; TORIYAMA SHIGETAKA; FUKUDA KAICHI
PA TOSHIBA CORP
PI JP 09092618 A 19970404 Heisei
AI JP 1995-246500 (JP07246500 Heisei) 19950925
PRAI JP 1995-246500 19950925
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To polycrystalize amorphous silicon efficiently by reducing reflection of a laser at the time of laser irradiation.
SOLUTION: A black **matrix** film 2 and an insulation film 3 are formed on a glass substrate 1 followed by formation of a display **pixel electrode** 8, a **source electrode** 6 and a **drain electrode** 7. Subsequently, a semiconductor of amorphous silicon, a first **silicon nitride** 14, a **silicon oxide** 15 and a second **silicon nitride** are deposited thereon. The semiconductor of amorphous silicon, the first **silicon nitride** 14, and the **silicon oxide** 15 are left at the part where the **gate electrode** 23 is not present. Phosphorus is then added from above the **silicon oxide** 15 at the part where the **gate electrode** 23 is not present by self-aligned technology using the **gate electrode** 23 as a mask thus converting a part of semiconductor of amorphous silicon into an n-type amorphous silicon. Upper surface of the **silicon oxide** 15 is then irradiated with laser light thus converting the n-type amorphous silicon added with phosphorus on which the **gate electrode** 23 is not present into n-type polysilicon.

L71 ANSWER 50 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1996-313934 JAPIO
TI ARRAY SUBSTRATE, ITS PRODUCTION, **LIQUID CRYSTAL** DISPLAY DEVICE AND ITS PRODUCTION
IN MIURA YASUNORI; KATSUKADO RAMESHIYU; SHIBUSAWA MAKOTO; HONJO MASUSHI; JINNAI NORIHIDE
PA TOSHIBA CORP
PI JP 08313934 A 19961129 Heisei
AI JP 1995-122452 (JP07122452 Heisei) 19950522
PRAI JP 1995-122452 19950522
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To provide a **liquid crystal** display device with which production stages are decreased without degrading its performance or without degrading its yield.
CONSTITUTION: **Gate electrodes** 2 are formed on one main surface of a glass substrate 1 and a gate insulating film 5 consisting of **silicon oxide** is formed. A high-resistance i-type amorphous silicon layer 6 is formed on the gate insulating film 5 corresponding to the **gate electrodes** 2 and low-resistance n-type polycrystalline silicon layers 7, 8 are formed adjacently thereto. **Source electrodes** 13 and **drain electrodes** 14 are formed by laminating transparent conductive films 11 consisting of ITO and molybdenum layers 12. Display

pixel electrodes 15 are formed by extending the transparent conductive films 11 on the **source electrode** 13 side. A protective insulating film 18 consisting of **silicon nitride** is formed on thin-film transistors 17 over the entire surface, by which a **matrix** array substrate 19 is constituted. Color filters 22 and counter electrodes 23 are laminated and formed on the glass substrate 21 and a counter substrate 24 is formed. **Liquid crystals** 29 are enclosed and held between the **matrix** array substrate 19 and the counter substrate 24.

L71 ANSWER 51 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1996-248444 JAPIO
TI DISPLAY PANEL
IN KOJIMA HIDETSUGU
PA CASIO COMPUT CO LTD
PI JP 08248444 A 19960927 Heisei
AI JP 1995-72479 (JP07072479 Heisei) 19950307
PRAI JP 1995-72479 19950307
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To decrease the parasitic capacitances between signal lines and **pixel electrodes** of an active **matrix** type **liquid crystal** display device without lowering an **opening** rate.
CONSTITUTION: Semiconductor thin films 31 and insulating films 32 are disposed in this order under signal lines 3 arranged along one side edge of the **pixel electrodes** 5 and atop gate insulating films 8. These semiconductor thin films 31 are formed simultaneously with the formation of semiconductor thin films 9 consisting of amorphous silicon of thin-film transistors(TFTs) 4. The insulating films 32 are formed simultaneously with the formation of channel protective films 10 consisting of **silicon oxide** or **silicon nitride** of these TFTs 4. The substantial spaces of the signal lines 3 and the **pixel electrodes** 5 are large without enlarging the spaces of the signal lines 3 and the **pixel electrodes** 5 in the horizontal direction in such a formation.

L71 ANSWER 52 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1995-168170 JAPIO
TI **LIQUID CRYSTAL** DISPLAY DEVICE
IN FURUSHIMA TERUHIKO
PA CANON INC
PI JP 07168170 A 19950704 Heisei
AI JP 1993-342819 (JP05342819 Heisei) 19931216
PRAI JP 1993-342819 19931216
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995
AB PURPOSE: To suppress the irregular orientation and the occuerence of discrimination due to the step on the surface of an element substrate having an electric element in an active-**matrix** liq. crystal display device and to form a picture of high definition and grade by making a liq. crystal layer on a **pixel electrode** region thinner than the liq. crystal layer on the other regions.
CONSTITUTION: A porous Si substrate 1 is used as a display substrate, and a single-crystal Si thin film epitaxially grown on the substrate is used as the active layer of a thin-film transistor. A transparent member 9 of **SiO**<SB>2</SB> is formed on the element substrate so that the part on which a **pixel electrode** 7 is formed is higher than the other parts, and then the electrode 7 of ITO and a passivation film 10 of **SiN**<SB>4</SB> are formed. A counter substrate is constituted by forming a light-shielding layer on a substrate 14 of a low thermal

expansion glass, further forming a color filter 13 of RGB, then forming a flattening film 12 and finally forming a counter electrode 11 of ITO.
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L71 ANSWER 53 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1995-159772 JAPIO
TI **LIQUID CRYSTAL** DISPLAY DEVICE
IN FURUSHIMA TERUHIKO
PA CANON INC
PI JP 07159772 A 19950623 Heisei
AI JP 1993-338992 (JP05338992 Heisei) 19931203
PRAI JP 1993-338992 19931203
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995
AB PURPOSE: To enable reduction in margin of the black **matrix**, a wider **opening** ratio and high definition and high contrast display by directly forming a color filter layer consisting of the color filters and the black **matrix** on the TFT substrate.
CONSTITUTION: A single crystal Si thin film formed on the porous Si substrate 1, as the TFT substrate, by the epitaxial growth method is used as the active layer of the thin film transistor. Then an inorganic transparent member consisting of **SiO**<SB>2</SB> is formed on the resulting TFT substrate and thereafter the picture element electrodes 7 consisting of ITO and the passivation film 10 consisting of **SiN** <SB>x</SB> are formed successively on it. Subsequently, the black **matrix** 11 consisting of Cr is formed on the passivation film 10 and the RGB color filters 12 are formed on the regions of the passivation film 10 on the picture element electrodes 7. Further, the flatening film 13 consisting of polyimide is formed. The counter-substrate is obtained by forming the counter-electrode 14 consisting of an ITO film on the glass substrate 16 and thereafter forming the oriented film 15 consisting of polyimide on it.
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L71 ANSWER 54 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1994-214253 JAPIO
TI **LIQUID CRYSTAL** DISPLAY DEVICE
IN ORITSUKI RYOJI; MATSUMARU HARUO; HORII JUICHI; HASHIMOTO YUICHI; SAKUTA HIROKI
PA HITACHI LTD
PI JP 06214253 A 19940805 Heisei
AI JP 1993-4723 (JP05004723 Heisei) 19930114
PRAI JP 1993-4723 19930114
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To prevent the generation of edge domains and an increase in off current by a photocontact and to provide the **liquid crystal** display device having excellent display characteristics by forming silicon films on protective films.
CONSTITUTION: Thin-film transistors TFT and transparent **pixel electrodes** ITO 1 are formed on a lower transparent glass substrate SUB 1 side with a **liquid crystal** LC as a reference.
Color filters FIL and light shielding films BM of black **matrix** patterns are formed on an upper transparent glass substrate SUB 2 side.
Silicon oxide films **SiO** formed by a dipping treatment, etc., are provided on both surfaces of the substrates SUB 1, SUB 2. Since the sharp flaws, if any, on the surfaces of the substrates SUB 1, SUB 2 are covered by the **silicon oxide** films **Sin**, the quality of the films such as scanning signal lines GL and light shielding films BM, deposited thereon is uniformly maintained.
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L71 ANSWER 55 OF 63 JAPIO COPYRIGHT 2003 JPO

AN 1994-085255 JAPIO
TI THIN FILM TRANSISTOR AND MANUFACTURE THEREOF
IN YAMAMOTO TOMOHIKO; SHIMADA YASUNORI
PA SHARP CORP
PI JP 06085255 A 19940325 Heisei
AI JP 1992-234977 (JP04234977 Heisei) 19920902
PRAI JP 1992-234977 19920902
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To provide a thin film transistor and a manufacture thereof preferably used in an active **matrix** substrate of a **liquid crystal** display with a large screen and a high fineness.
CONSTITUTION: An insulating film 3 made of AlN is formed so as to cover a **gate electrode** wiring 2 made of Al or alloy containing Al formed on an insulating substrate 1. An insulating film 4 made of **SiN**<SB>x</SB> or **SiO**<SB>2</SB> is formed on the insulating film 3. Since the resistivity of Al is small, the electrode wiring having the low resistance can be formed. The insulating film 3 made of AlN can be formed by a sputtering or by implanting an ion shower containing nitrogen on the surface of Al or alloy containing Al. Thus, the non-porous, thick insulating film 3 made of AlN with thick high mechanical strength is easily formed, and thereby the insulating failure of the **gate electrode** wiring 2 with a **source electrode** wiring 8b and a **drain electrode** 8a does not, occur, and a good insulating layer can be formed.

L71 ANSWER 56 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1992-280230 JAPIO
TI ACTIVE **MATRIX** TYPE **LIQUID CRYSTAL** DISPLAY ELEMENT
IN FUKUDA KAICHI
PA TOSHIBA CORP
PI JP 04280230 A 19921006 Heisei
AI JP 1991-43301 (JP03043301 Heisei) 19910308
PRAI JP 1991-43301 19910308
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992
AB PURPOSE: To simplify the manufacturing process by forming an insulating layer and a two-layered gate insulating film from a material of the same kind.
CONSTITUTION: A transparent auxiliary capacity electrode 2 is formed on one main surface of a transparent insulating base plate 1, and an insulating layer 3 consisting of a **silicon oxide** film is formed as a layer-to-layer insulating film so as to cover the electrode 2. A **gate electrode** 4 is formed on the insulating film 3, and a first gate insulating film 5 consisting of silicone oxide is formed as the first layer of a gate insulating film so as to cover the **gate electrode** 4. A transparent picture element electrode 6 is formed on the first gate insulating film 5. A gate insulating film 7 consisting of a **silicon oxide** film and a third gate insulating film 7 consisting of a **silicon nitride** film are successively formed as the second and third layers of the gate insulating film so as to cover the transparent electrode 6. Then, a semiconductor film 8, an inorganic protective film 10 consisting of a **silicon nitride** film, and further a semiconductor film 11 are formed on the third gate insulating film 8.

L71 ANSWER 57 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1992-037822 JAPIO
TI ACTIVE **MATRIX** TYPE DISPLAY DEVICE AND ITS PRODUCTION

IN MITANI YASUHIRO; INAMI TAKASHI
PA SHARP CORP
PI JP 04037822 A 19920207 Heisei
AI JP 1990-146856 (JP02146856 Heisei) 19900604
PRAI JP 1990-146856 19900604
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992
AB PURPOSE: To obtain an active **matrix** type display element having high aperture by forming a picture element electrode between plural gate bus wires and between plural source bus wires so as not to generate a gap. CONSTITUTION: After depositing Ta on a glass base 1, gate bus wires 11 and **gate electrodes** 2 are patterned, a gate insulating film 3 consisting of SiNX is formed so as to cover the gate pattern and then an a-Si layer is deposited to form a semiconductor layer 4. Then, a P (phosphorus) doped a-**Si**(**n**<SP>+</SP>) layer is deposited on the layer 4 to form **contact** layers 5a, 5b. Then a Ti or Mo metallic layer is formed to form source bus wires 12 and **source electrodes** 6. Then, an inter-layer insulating layer 8 consisting of SinX or **SiO**<SB>2</SB>, or both of them is formed so as to cover a TFT 13 formed by said method and then a transparent conductive film consisting of silver indium oxide is deposited on the base to form the picture element electrode 9. Then, an oriented film or the like is formed to complete an active **matrix** base and **liquid crystal** is sealed between the base and a counter base to complete the active **matrix** type display element. COPYRIGHT: (C)1992,JPO&Japio

L71 ANSWER 58 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1992-012330 JAPIO
TI ACTIVE **MATRIX** TYPE **LIQUID CRYSTAL** DISPLAY DEVICE
IN KOBAYASHI KEIZO
PA NEC CORP
PI JP 04012330 A 19920116 Heisei
AI JP 1990-112639 (JP02112639 Heisei) 19900430
PRAI JP 1990-112639 19900430
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992
AB PURPOSE: To prevent cracking, film peeling, etc., and to improve barrier effect against alkali ions by varying the composition of the silicon oxynitride film of a surface protective film gently from the **silicon oxide** film side to the **silicon nitride** film side. CONSTITUTION: The surface protective film 20 on a back channel which is buried by **etching** is formed in three-layered structure of a **silicon oxide** film 21, a silicon oxynitride film 22, and a **silicon nitride** film 23. Then the composition of the silicon oxynitride film 22 is varied gently from the side of the **silicon oxide** film 21 to the side of the **silicon nitride** film 23. Consequently, the localization of an interface potential which is seen on a conventional **SiO**<SB>2</SB>-S<SB>i3</SB>N<SB>4</SB> interface is eliminated and small film stress and film thickness reduction are realized; and there is no possibility of film peeling and the uppermost part is formed of the **silicon nitride** film, so the barrier effect against contamination by and intrusion of alkali ions becomes sufficient. COPYRIGHT: (C)1992,JPO&Japio

L71 ANSWER 59 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1989-291467 JAPIO
TI THIN FILM TRANSISTOR
IN DOJIRO MASAYUKI; IKEDA MITSUSHI; OANA YASUHISA
PA TOSHIBA CORP

PI JP 01291467 A 19891124 Heisei
AI JP 1988-122771 (JP63122771 Showa) 19880519
PRAI JP 1988-122771 19880519
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To improve the performance of a thin film transistor(TFT) by forming the **gate electrode** material of the TFT of a structure in which a **gate electrode** is disposed under a semiconductor film of a Mo-Ta alloy film containing a composition of a predetermined range, and forming a gate insulating film of a composite structure of the oxide film of the **gate electrode** and a **silicon nitride** film.
CONSTITUTION: A glass substrate 1 is employed as an insulating substrate, and a **gate electrode** 2 of a Mo-Ta alloy film is patterned and formed thereon. The electrode 2 is patterned in one direction and formed as address wirings in case of an active **matrix** substrate. The alloy film contains 60 to 85 atomic % of Ta. A gate insulating film formed of a composite film of an oxide film 3 obtained by anodizing the electrode 3, a **silicon oxide** film 4 and a **silicon nitride** film 5 is formed on the surface of the electrode 2. Thus, the TFT having high performance is obtained, and a **liquid crystal** display device having a large area, precise accuracy and high reliability can be formed.

L71 ANSWER 60 OF 63 JAPIO
AN 1989-276671 JAPIO
TI STAGGERED TOP TYPE AMORPHOUS SILICON THIN FILM TRANSISTOR
IN TANAKA SAKAE; WATANABE YOSHIAKI; SHIRAI KATSUO
PA SEIKOSHA CO LTD
NIPPON PRECISION CIRCUITS KK
PI JP 01276671 A 19891107 Heisei
AI JP 1988-105280 (JP63105280 Showa) 19880427
PRAI JP 1988-105280 19880427
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To eliminate crackings by a method wherein a **silicon nitride** layer is formed on an amorphous silicon layer and a **silicon oxide** layer is formed on the **silicon nitride** layer.
CONSTITUTION: A **silicon nitride** layer 7 is formed on an amorphous silicon layer 6 as a gate insulating layer and a **silicon oxide** layer 8 is formed on the **silicon nitride** layer 7. Or, the **silicon oxide** layer 8 is formed on the amorphous silicon layer 6 and the **silicon nitride** layer 7 is formed on the **silicon oxide** layer 8. Therefore, the stress in the **silicon nitride** layer 7 is relieved by the **silicon oxide** layer 8. With this constitution, crackings can be eliminated and the yield is improved significantly. Especially, if this structure is applied to the amorphous silicon thin film transistor of an active **matrix** type **liquid crystal** display, the penetration of **etchant** which occurs when a **gate electrode** is **etched** can be avoided, so that the possibility of corrosion of a picture element electrode can be eliminated.

L71 ANSWER 61 OF 63 JAPIO
AN 1989-022066 JAPIO
TI THIN FILM TRANSISTOR
IN SUZUKI KOJI; OTAGURO HIROSHI; AKIYAMA MASAHIKO; TOEDA HISAO
PA TOSHIBA CORP
PI JP 01022066 A 19890125 Heisei

AI JP 1987-178397 (JP62178397 Showa) 19870717
PRAI JP 1987-178397 19870717
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To reduce the leak current for light incidence from **gate electrode** side without deteriorating other element characteristics, by a method wherein, in a thin film transistor used in an active **matrix** type **liquid crystal** display device and the like, patterning is performed in the manner in which a specified amount of a semiconductor thin film protrudes in the direction of current flow from an electrode edge.
CONSTITUTION: On a substrate on which a **gate electrode** 2 and an address wiring 3 are formed, an a-Si: H film 5 is formed in a specified pattern, **via** a gate insulating film 4, which is, e.g., one of **SiO**<SB>x</SB> and **SiN**<SB>x</SB>, or a lamination film of them. The a-Si: H film 5 is an undoped high resistance film of about 300nm in thickness, on which **source.drain electrodes** 7, 8 are formed **via** an N-type a-Si: H film 6<SB>1</SB>, 6<SB>2</SB>. The electrodes 7, 8 and a data wiring 9 are made of an Al film, and a display electrode 10 composed of a transparent conductive film is formed on a picture element region. On the a-Si: H film, a pattern is formed so as to protrude with d (μm) from an edge of the **gate electrode** 2, in the width direction of the **gate electrode** 2, e.g., the current path direction of a transistor. The amount of protruding (d) is 0<d<=4.
COPYRIGHT: (C)1989,JPO&Japio

L71 ANSWER 62 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1987-245221 JAPIO
TI ACTIVE **MATRIX LIQUID CRYSTAL** PANEL
IN NOMOTO TSUTOMU; NISHIKI TAMAHIKO
PA OKI ELECTRIC IND CO LTD
PI JP 62245221 A 19871026 Showa
AI JP 1986-88190 (JP61088190 Showa) 19860418
PRAI JP 1986-88190 19860418
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1987
AB PURPOSE: To uniform the gap between substrates where a **liquid crystal** should be charged to attain an excellent display quality by providing an insulating layer on at least one of faces facing each other of the first and second light- transmissive insulating substrates in an area corresponding to a display electrode.
CONSTITUTION: A film consisting of a **silicon oxide**, a **silicon nitride**, or the like is formed on the first light-transmissive insulating substrate 11 consisting of glass, quartz, or the like with a film thickness approximately equal to the height from the surface of the first substrate 11 to the upper face of a TFT 15. This film is so worked by the photoetching technique that the film remains with the same area as a display electrode 13, thus obtaining an insulating layer 51. A transparent conductive film is formed on the first substrate 11 including this insulating film 51 and is worked by **etching** to form the display electrode 13 on the insulating layer 51, and thus, the TFT 15 as a switching element is formed. In this case, the area of the part, which is formed on the display electrode 13, of a **source electrode** 25 is narrowed within the range where they are surely connected electrically.
COPYRIGHT: (C)1987,JPO&Japio

L71 ANSWER 63 OF 63 JAPIO COPYRIGHT 2003 JPO
AN 1986-260219 JAPIO
TI **LIQUID CRYSTAL** DISPLAY DEVICE
IN SUZUKI TERUYA
PA SEIKO INSTR & ELECTRONICS LTD

03/25/2003

PI JP 61260219 A 19861118 Showa
AI JP 1985-103141 (JP60103141 Showa) 19850515
PRAI JP 1985-103141 19850515
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1986
AB PURPOSE: To make an easy to produce the titled device, and to improve the trust of the titled device by forming a non-linear resistance element composed of an amorphous material contg. silicon as a main component in a series with the **liquid crystal** for each picture element of the electrode for operating the **liquid crystal**.

CONSTITUTION: The amorphous material 3 composed of silicon as the main component, is formed according to the plasma CVD method to the film having 1,000Å in thickness, using a silane gas and a mixed gas contg. a carbon dioxide, a nitrous oxide and an oxygen gas, when forming the **silicon oxide** film, and a mixed gas contg. an ammonia gas and a nitrogen gas, when forming the **silicon nitride** . The metal electrode 4 forms one side of the electrodes in the **matrix** electrode, and is formed by sputtering a metallic chromium in 3,000Å in thickness on the substrate. Al, Cu, Ni, Cr, Ag, and Ta etc. may be used in addition to Cr. And then, the metal electrode 4 is selectively removed by photoetching, followed by selectively removing the amorphous film 3 composed of the silicon as the main component with **etching**, without removing a photosensitive resin. As a result, the substrate composed of the non-linear resistance element is formed by photomasking two times, and by **etching** three times.

L73 ANSWER 1 OF 5 WPIX (C) 2003 THOMSON DERWENT
AN 1995-165435 [22] WPIX
CR 1994-187226 [23]; 1994-187227 [23]; 1999-333479 [28]; 2000-434915 [37]; 2001-296716 [31]; 2002-321843 [24]
DNN N2001-082809 DNC C2001-033668
TI Thin film transistor manufacturing method for **LCD** device, image sensor, involves forming gate electrodes by nitriding surface of **silicon oxide** film having chlorine.
DC L03 P81 P85 U11 U12 U14
IN YAMAZAKI, S; **ZHANG, H**
PA (SEME) SEMICONDUCTOR ENERGY LAB; (SEME) SEMICONDUCTOR ENERGY LAB CO LTD
CYC 4
PI JP 07086593 A 19950331 (199522)* 5p
KR 131062 B1 19980414 (200011)
CN 1248037 A 20000322 (200032)
CN 1248069 A 20000322 (200032)
US 6168980 B1 20010102 (200113)B 19p
ADT JP 07086593 A JP 1993-177410 19930624; KR 131062 B1 KR 1993-16789 19930827; CN 1248037 A Div ex CN 1993-118309 19930827, CN 1999-111870 19930827; CN 1248069 A Div ex CN 1993-118309 19930827, CN 1999-111869 19930827; US 6168980 B1 Cont of US 1993-111522 19930825, US 1996-721526 19960926
PRAI JP 1993-177410 19930624; JP 1992-252296 19920827; JP 1993-191934 19930706
AB US 6168980 B UPAB: 20010307 ABEQ treated as Basic
NOVELTY - Crystallization of silicon film on substrate is promoted by diffusion of metal selected from specific group. The active layer is formed by patterning the silicon film. A **silicon oxide** film containing chlorine is formed on active layer by chemical vapor deposition. The gate electrodes are formed on **silicon oxide** film by nitriding surface of **silicon oxide** film.

DETAILED DESCRIPTION - Crystallization of silicon film formed on substrate is promoted by diffusion of metal selected from group of nickel, iron, cobalt, ruthenium, rhodium, palladium, osmium, iridium, platinum, scandium, titanium, vanadium, chromium, manganese, copper, zinc, gold and silver.

USE - For manufacture of NTFT, PTFT used in pixel electrode, peripheral circuit of **LCD** device, driver circuit of image sensor, microprocessor, microcontroller, microcomputer, memory.

ADVANTAGE - Improves yield of reliable and excellent TFT at manufacturing temperature of 700 deg. C or less. Improves characteristic of insulator by increasing dielectric constant of film. Avoids stagnation of fixed charge inside gate insulator and static breakdown and pin holes by increasing density of gate insulator. Facilitates formation of 3D IC by superimposing IC on single crystal IC.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of manufacturing process of TFT.

Dwg.4C/7

AB JP 07086593 A UPAB: 20020610
The manufacturing method involves formation of a **silicon oxide** film as a gate insulating film (13) over a glass substrate (11). Nitrogen ions are poured into this gate insulating film. Subsequent annealing is performed through IR irradiation. Now this gate insulating film is transformed into an oxide of **silicon nitride**.

USE DVANTAGE - For use in **LCD** device. Stabilizes TFT characteristics. Raises breakdown voltage and dielectric constant. Realizes high precision quality film formation. Raises reliability of operation.

Dwg.1/3

L73 ANSWER 2 OF 5 WPIX (C) 2003 THOMSON DERWENT
AN 1994-228666 [28] WPIX
CR 1992-286104 [35]; 1993-186082 [23]; 1993-381162 [48]; 1994-010822 [02]; 1994-010823 [02]; 1994-016802 [03]; 1994-038407 [05]; 1994-068409 [09]; 1994-069941 [09]; 1994-297831 [37]; 1994-352611 [44]; 1994-352612 [44]; 1996-458685 [46]; 1998-185671 [17]; 1999-067035 [06]; 1999-112307 [10]; 1999-127636 [11]; 1999-410731 [35]; 2000-132661 [12]; 2000-187992 [17]; 2000-275998 [24]; 2001-215164 [22]; 2002-323093 [36]; 2002-422617 [45]
DNN N1994-180544 DNC C1994-104562
TI Insulation gate-type semiconductor device preventing movable ion invasion - comprises a semiconductor insulation film and aluminium gate electrode on an insulating substrate.
DC L03 P81 U11 U12 U14
IN TAKAMURA, Y; YAMAZAKI, S; **ZHANG, H**; TAKEMURA, Y
PA (SEME) SEMICONDUCTOR ENERGY LAB; (SEME) HANDOTAI ENERGY KENKYUSHO KK
CYC 4
PI JP 06163896 A 19940610 (199428)* 6p
CN 1081022 A 19940119 (199712)
US 5879969 A 19990309 (199917)
US 5917225 A 19990629 (199932)
KR 123795 B1 19971125 (199950)
KR 139321 B1 19980715 (200018)
KR 139322 B1 19980715 (200018)
ADT JP 06163896 A JP 1992-102202 19920327; CN 1081022 A CN 1993-104560 19930327; US 5879969 A CIP of US 1992-846164 19920305, Div ex US 1993-37162 19930325, Cont of US 1995-460560 19950602, US 1997-841638 19970430; US 5917225 A CIP of US 1992-846164 19920305, Div ex US 1993-37162 19930325, Div ex US 1995-460560 19950602, US 1996-721052 19960926; KR 123795 B1 KR 1993-4800 19930326; KR 139321 B1 Div ex KR 1993-4800 19930326, KR 1997-23073 19970604; KR 139322 B1 Div ex KR 1993-4800 19930326, KR 1997-23074 19970604
FDT US 5879969 A CIP of US 5289030, Div ex US 5468987; US 5917225 A CIP of US 5289030, Div ex US 5468987
PRAI JP 1992-102202 19920327; JP 1992-113027 19920406; JP 1992-124324 19920417
AB US 5468987 A UPAB: 19960108 ABEQ treated as Basic
The insulated gate thin film transistor comprises a semiconductor layer formed on an insulating surface having source, drain and channel regions in it. A first insulating layer is provided on the semiconductor layer. A second insulating layer is located over the channel region with the first insulating layer between them, the second insulating layer having opposed side edges. A gate electrode is located over the channel region with the first insulating layer and the second insulating layer interposed between them. An anodic oxide coating covers a surface of the gate electrode, the oxide coating being formed by anodic oxidizing a surface of the gate electrode.

The first insulating layer extends beyond the side edges of the second insulating layer to cover a major surface of the source and drain regions. The side edges of the second insulating layer are approximately coextensive with edges of the anodic oxide coating. The insulating layers comprise aluminium oxide, **silicon nitride**, **silicon oxide** or phospho-silicate glass.

USE/ADVANTAGE - E.g. for **liquid crystal** display. Over-etching is suppressed to prevent diffusion of foreign elements from substrate. Improved flatness.

Dwg.7/14
AB JP 06163896 A UPAB: 20020717
Semiconductor layer, insulation film layer of **silicon oxide** layer and a **silicon nitride** layer and gate electrode of aluminium are formed on an insulating substrate.

USE - An invasion of movable ion is prevented.
Dwg.0/3

L73 ANSWER 3 OF 5 WPIX (C) 2003 THOMSON DERWENT
AN 1994-069941 [09] WPIX
CR 1992-286104 [35]; 1993-186082 [23]; 1993-381162 [48]; 1994-010822 [02]; 1994-010823 [02]; 1994-016802 [03]; 1994-038407 [05]; 1994-068409 [09]; 1994-228666 [28]; 1994-297831 [37]; 1994-352611 [44]; 1994-352612 [44]; 1996-458685 [46]; 1998-185671 [17]; 1999-067035 [06]; 1999-112307 [10]; 1999-127636 [11]; 1999-410731 [35]; 2000-132661 [12]; 2000-187992 [17]; 2000-275998 [24]; 2001-215164 [22]; 2002-323093 [36]; 2002-422617 [45]
DNN N1996-000015 DNC C1996-000005
TI Thin film insulated gate field effect transistor - has portion of gate electrode coated with metal material such as chrome, and removed with anodic oxide.
DC L03 P81 U11 U12 U14
IN TAKAMURA, Y; YAMAZAKI, S; **ZHANG, H**; TAKEMURA, Y
PA (SEME) SEMICONDUCTOR ENERGY LAB; (SEME) HANDOTAI ENERGY KENKYUSHO KK; (SEME) SEMICONDUCTOR ENERGY RES CO LTD
CYC 5
PI JP 06021465 A 19940128 (199409)* 6p
TW 223178 A 19940501 (199549)
US 5468987 A 19951121 (199601)B 20p
CN 1081022 A 19940119 (199712)
US 5879969 A 19990309 (199917)
US 5917225 A 19990629 (199932)
KR 123795 B1 19971125 (199950)
KR 139321 B1 19980715 (200018)
KR 139322 B1 19980715 (200018)
ADT JP 06021465 A JP 1993-103516 19930405; TW 223178 A TW 1992-105052 19920626; US 5468987 A CIP of US 1992-846164 19920305, US 1993-37162 19930325; CN 1081022 A CN 1993-104560 19930327; US 5879969 A CIP of US 1992-846164 19920305, Div ex US 1993-37162 19930325, Cont of US 1995-460560 19950602, US 1997-841638 19970430; US 5917225 A CIP of US 1992-846164 19920305, Div ex US 1993-37162 19930325, Div ex US 1995-460560 19950602, US 1996-721052 19960926; KR 123795 B1 KR 1993-4800 19930326; KR 139321 B1 Div ex KR 1993-4800 19930326, KR 1997-23073 19970604; KR 139322 B1 Div ex KR 1993-4800 19930326, KR 1997-23074 19970604
FDT US 5468987 A CIP of US 5289030; US 5879969 A CIP of US 5289030, Div ex US 5468987; US 5917225 A CIP of US 5289030, Div ex US 5468987
PRAI JP 1992-124324 19920417; JP 1992-102202 19920327; JP 1992-113027 19920406
AB US 5468987 A UPAB: 19960108 ABEQ treated as Basic
The insulated gate thin film transistor comprises a semiconductor layer formed on an insulating surface having source, drain and channel regions in it. A first insulating layer is provided on the semiconductor layer. A second insulating layer is located over the channel region with the first insulating layer between them, the second insulating layer having opposed side edges. A gate electrode is located over the channel region with the first insulating layer and the second insulating layer interposed between them. An anodic oxide coating covers a surface of the gate electrode, the oxide coating being formed by anodic oxidizing a surface of the gate electrode.

The first insulating layer extends beyond the side edges of the second insulating layer to cover a major surface of the source and drain regions. The side edges of the second insulating layer are approximately coextensive with edges of the anodic oxide coating. The insulating layers comprise aluminium oxide, **silicon nitride**, **silicon oxide** or phospho-silicate glass.

USE/ADVANTAGE - E.g. for **liquid crystal** display.
Over-etching is suppressed to prevent diffusion of foreign elements from

substrate. Improved flatness.
Dwg.7/14

AB JP 06021465 A UPAB: 20020717
The insulated gate thin film transistor comprises a semiconductor layer formed on an insulating surface having source, drain and channel regions in it. A first insulating layer is provided on the semiconductor layer. A second insulating layer is located over the channel region with the first insulating layer between them, the second insulating layer having opposed side edges. A gate electrode is located over the channel region with the first insulating layer and the second insulating layer interposed between them. An anodic oxide coating covers a surface of the gate electrode, the oxide coating being formed by anodic oxidizing a surface of the gate electrode.

The first insulating layer extends beyond the side edges of the second insulating layer to cover a major surface of the source and drain regions. The side edges of the second insulating layer are approximately coextensive with edges of the anodic oxide coating. The insulating layers comprise aluminium oxide, **silicon nitride**, **silicon oxide** or phospho-silicate glass.

USE/ADVANTAGE - E.g. for **liquid crystal** display.
Over-etching is suppressed to prevent diffusion of foreign elements from substrate. Improved flatness.
Dwg.1/5

L73 ANSWER 4 OF 5 WPIX (C) 2003 THOMSON DERWENT
AN 1994-068409 [09] WPIX
CR 1992-286104 [35]; 1993-186082 [23]; 1993-381162 [48]; 1994-010822 [02]; 1994-010823 [02]; 1994-016802 [03]; 1994-038407 [05]; 1994-069941 [09]; 1994-228666 [28]; 1994-297831 [37]; 1994-352611 [44]; 1994-352612 [44]; 1996-458685 [46]; 1998-185671 [17]; 1999-067035 [06]; 1999-112307 [10]; 1999-127636 [11]; 1999-410731 [35]; 2000-132661 [12]; 2000-187992 [17]; 2000-275998 [24]; 2001-215164 [22]; 2002-323093 [36]; 2002-422617 [45]
DNN N1994-053362 DNC C1994-030576
TI Thin film insulated gate field effect transistor - has portion of gate electrode coated with metal material such as chrome, and removed with anodic oxide.
DC L03 P81 U12
IN TAKAMURA, Y; YAMAZAKI, S; **ZHANG, H**
PA (SEME) SEMICONDUCTOR ENERGY LAB
CYC 1
PI JP 06013610 A 19940121 (199409)* 7p
ADT JP 06013610 A JP 1993-103515 19930405
PRAI JP 1992-113027 19920406
AB JP 06013610 A UPAB: 20020717
The insulated gate thin film transistor comprises a semiconductor layer formed on an insulating surface having source, drain and channel regions in it. A first insulating layer is provided on the semiconductor layer. A second insulating layer is located over the channel region with the first insulating layer between them, the second insulating layer having opposed side edges. A gate electrode is located over the channel region with the first insulating layer and the second insulating layer interposed between them. An anodic oxide coating covers a surface of the gate electrode, the oxide coating being formed by anodic oxidizing a surface of the gate electrode.

The first insulating layer extends beyond the side edges of the second insulating layer to cover a major surface of the source and drain regions. The side edges of the second insulating layer are approximately coextensive with edges of the anodic oxide coating. The insulating layers comprise aluminium oxide, **silicon nitride**, **silicon oxide** or phospho-silicate glass.

USE/ADVANTAGE - E.g. for **liquid crystal** display.

Over-etching is suppressed to prevent diffusion of foreign elements from substrate. Improved flatness.
Dwg.1/6

L73 ANSWER 5 OF 5 WPIX (C) 2003 THOMSON DERWENT
AN 1994-038407 [05] WPIX
CR 1992-286104 [35]; 1993-186082 [23]; 1993-381162 [48]; 1994-010822 [02]; 1994-010823 [02]; 1994-016802 [03]; 1994-068409 [09]; 1994-069941 [09]; 1994-228666 [28]; 1994-297831 [37]; 1994-352611 [44]; 1994-352612 [44]; 1996-458685 [46]; 1998-185671 [17]; 1999-067035 [06]; 1999-112307 [10]; 1999-127636 [11]; 1999-410731 [35]; 2000-132661 [12]; 2000-187992 [17]; 2000-275998 [24]; 2001-215164 [22]; 2002-323093 [36]; 2002-422617 [45]
DNN N1996-000015 DNC C1996-000005
TI Thin film insulated gate field effect transistor - has portion of gate electrode coated with metal material such as chrome, and removed with anodic oxide.
DC L03 P81 U11 U12 U14
IN TAKAMURA, Y; YAMAZAKI, S; **ZHANG, H**; TAKEMURA, Y
PA (SEME) SEMICONDUCTOR ENERGY LAB; (SEME) HANDOTAI ENERGY KENKYUSHO KK
CYC 4
PI JP 05343430 A 19931224 (199405)* 19p
CN 1081022 A 19940119 (199712)
US 5879969 A 19990309 (199917)
US 5917225 A 19990629 (199932)
KR 123795 B1 19971125 (199950)
KR 139321 B1 19980715 (200018)
KR 139322 B1 19980715 (200018)
ADT JP 05343430 A JP 1992-187604 19920622; CN 1081022 A CN 1993-104560 19930327; US 5879969 A CIP of US 1992-846164 19920305, Div ex US 1993-37162 19930325, Cont of US 1995-460560 19950602, US 1997-841638 19970430; US 5917225 A CIP of US 1992-846164 19920305, Div ex US 1993-37162 19930325, Div ex US 1995-460560 19950602, US 1996-721052 19960926; KR 123795 B1 KR 1993-4800 19930326; KR 139321 B1 Div ex KR 1993-4800 19930326, KR 1997-23073 19970604; KR 139322 B1 Div ex KR 1993-4800 19930326, KR 1997-23074 19970604
FDT US 5879969 A CIP of US 5289030, Div ex US 5468987; US 5917225 A CIP of US 5289030, Div ex US 5468987
PRAI JP 1992-113027 19920406; JP 1991-237100 19910823; JP 1991-238713 19910826; JP 1992-102202 19920327; JP 1992-124324 19920417
AB US 5468987 A UPAB: 19960108 ABEQ treated as Basic
The insulated gate thin film transistor comprises a semiconductor layer formed on an insulating surface having source, drain and channel regions in it. A first insulating layer is provided on the semiconductor layer. A second insulating layer is located over the channel region with the first insulating layer between them, the second insulating layer having opposed side edges. A gate electrode is located over the channel region with the first insulating layer and the second insulating layer interposed between them. An anodic oxide coating covers a surface of the gate electrode, the oxide coating being formed by anodic oxidizing a surface of the gate electrode.

The first insulating layer extends beyond the side edges of the second insulating layer to cover a major surface of the source and drain regions. The side edges of the second insulating layer are approximately coextensive with edges of the anodic oxide coating. The insulating layers comprise aluminium oxide, **silicon nitride**, **silicon oxide** or phospho-silicate glass.

USE/ADVANTAGE - E.g. for **liquid crystal** display.
Over-etching is suppressed to prevent diffusion of foreign elements from substrate. Improved flatness.
Dwg.7/14
AB JP 05343430 A UPAB: 20020717

The insulated gate thin film transistor comprises a semiconductor layer formed on an insulating surface having source, drain and channel regions in it. A first insulating layer is provided on the semiconductor layer. A second insulating layer is located over the channel region with the first insulating layer between them, the second insulating layer having opposed side edges. A gate electrode is located over the channel region with the first insulating layer and the second insulating layer interposed between them. An anodic oxide coating covers a surface of the gate electrode, the oxide coating being formed by anodic oxidizing a surface of the gate electrode.

The first insulating layer extends beyond the side edges of the second insulating layer to cover a major surface of the source and drain regions. The side edges of the second insulating layer are approximately coextensive with edges of the anodic oxide coating. The insulating layers comprise aluminium oxide, **silicon nitride**, **silicon oxide** or phospho-silicate glass.

USE/ADVANTAGE - E.g. for **liquid crystal** display. Over-etching is suppressed to prevent diffusion of foreign elements from substrate. Improved flatness.

Dwg.1/21

FILE 'REGISTRY'

L1 1 S SILICON NITRIDE/CN
L2 2 S SILICON OXIDE/CN
L3 1 S SILICON DIOXIDE/CN
L4 0 S NSI/CN
L5 0 S SIN/CN
L6 6 S NSI/MF
L7 13 S OSI/MF

FILE 'HCAPLUS'

L8 115482 S LCD OR LC(W)DISPLAY? OR LIQUID(W)CRYSTAL
L9 413474 S MATRIX OR MATRICES OR MATRIXES
L10 6442 S (MULTILEVEL OR MULTI(W)LEVEL OR MULTILAYER? OR MULTI(W)LAYER)(4A)(INSULAT? OR DIELECTRIC)
L11 76524 S (SILICON)(W)(NITRIDE OR MONONITRIDE) OR SIN OR SI(W)N
L12 443217 S (SILICON)(W)(DIOXIDE OR MONOOXIDE) OR SIO OR SI(W)O OR SILICON(W)OXIDE OR SILICA
L13 16458 S GATE(W)ELECTRODE
L14 2811 S PIXEL(W)ELECTRODE
L15 6216 S (SOURCE OR DRAIN)(2A)(ELECTRODE)
L16 1395749 S CONTACT OR OPEN? OR VIA OR HOLE
L17 170071 S ETCH###
L18 8603 S L8 AND L9
L19 245 S L18 AND (L1 OR L6) AND (L2 OR L3 OR L7)
L20 245 S L19 AND L9
L21 21 S L20 AND L14
L22 27 S L20 AND L13
L23 4 S L20 AND L10
L24 19 S L20 AND L15
L25 9 S L20 AND L16 AND L17
L26 629 S L8 AND L11 AND L12
L27 272 S L26 AND L9
L28 26 S L27 AND L14
L29 31 S L27 AND L13
L30 5 S L27 AND L10
L31 21 S L27 AND L15
L32 10 S L27 AND L16 AND L17
L33 52 S L21 OR L22 OR L23 OR L24 OR L25
L34 11 S (L28 OR L29 OR L30 OR L31 OR L32) NOT (L21 OR L22 OR L23 OR L24 OR L25)
L35 424 S L18 AND L17
L36 424 S L35 AND L9
L37 2088 S L8 AND L17
L38 424 S L37 AND L9
L39 118 S L38 AND L16

L40 2 S L39 AND L10
L41 31 S L39 AND L13
L42 28 S L39 AND L14
L43 31 S L39 AND L15
L44 46 S (L40 OR L41 OR L42) NOT (L28 OR L29 OR L30 OR L31 OR L32 OR L21 OR L22 OR L23 OR L24 OR L25)
L45 0 S L44 AND (L11 OR L1 OR L6) AND (L2 OR L3 OR L12)
L46 63 S L28 OR L29 OR L30 OR L31 OR L32 OR L21 OR L22 OR L23 OR L24 OR L25
SEL PN
L47 66 S (EP837355/PN OR EP1071124/PN OR EP647971/PN OR EP768710/PN OR EP813251/PN OR JP05011271/PN OR "JP2864794 B2"/PN OR US5414278/PN OR WO9930369/PN OR CN1184954/PN OR CN1282107/PN OR EP974164/PN OR JP02260661/PN OR JP03080226/PN OR JP04012330/PN OR JP04163528/PN OR JP04264774/PN OR JP05181158/PN OR JP05297409/PN OR "JP06044625 B4"/PN OR JP06130421/PN OR JP06194688/PN OR JP07094753/PN OR JP07254710/PN OR JP07263703/PN OR JP07270821/PN OR JP07273342/PN OR JP08018064/PN OR JP08029808/PN OR JP08097432/PN OR JP08116066/PN OR JP08122813/PN OR JP08220558/PN OR JP08241892/PN OR JP08255875/PN OR JP09148329/PN OR JP09197436/PN OR JP09213968/PN OR JP09230348/PN OR JP09246558/PN OR JP09252136/PN OR JP09283492/PN OR JP10010583/PN OR JP10062797/PN OR JP10135465/PN OR JP10177181/PN OR JP10189990/PN OR JP10239698/PN OR JP11045879/PN OR JP11097714/PN OR JP11126038/PN OR JP11133892/PN OR JP11202368/PN OR JP11326941/PN OR JP2000012863/PN OR JP2000267595/PN OR JP2000269504/PN OR JP2001015760/PN OR JP2001028439/PN OR JP2001035808/PN OR JP2001083895/PN OR JP2001125134/PN OR JP2001174818/PN OR JP2001255554/PN OR JP2001282139/PN OR JP2001511317/PN OR JP2002252353/PN OR JP2002305306/PN OR JP2002323706/PN OR "JP2508851 B2"/PN OR "JP2536230 B2"/PN OR "JP2963529 B2"/PN OR "JP3105408 B2"/PN OR "JP3182351 B2"/PN OR "JP3199311 B2"/PN OR "JP3230659 B2"/PN OR "JP3249077 B2"/PN OR "JP3270674 B2"/PN OR "JP3358284 B2"/PN OR KR133863/PN OR KR133864/PN OR TW441133/PN OR TW448332/PN OR TW469420/PN OR TW473639/PN OR US2001005020/PN OR US2001010566/PN OR US20020006
13/PN OR US2002012080/PN OR US2002021403/PN OR US2002027622/PN OR US2002055206/PN OR US2002063835/PN OR US2002117719/PN OR US2002126233/PN OR US2002145143/PN OR US2002159016/PN OR US5060036/PN OR US5191453/PN OR US5300449/PN OR US5563432/PN OR US5612234/PN OR US5728592/PN OR US5767530/PN OR US5814529/PN
OR US5899548/PN OR US5905548/PN OR US5940732/PN OR US5994173/P

L51 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:731440 HCAPLUS
DN 127:365090
TI Thin-film transistor and its fabrication
IN **Zhang, Hongyong**; Teramoto, Satoshi
PA Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09283518	A2	19971031	JP 1996-115672	19960412
PRAI	JP 1996-115672		19960412		

AB The invention relates to a TFT, suite for use in an active matrix **liq. crystal** display, wherein the interlayer insulating film is consists of **silicon nitride** having specified value of the inner stress, for reliable etching, and prevention of hydrogen desorption from the active layer.

L33 ANSWER 1 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:778448 HCAPLUS
DN 137:286613
TI Active **matrix liquid crystal** display device using thin film transistor
IN Kawasaki, Masahiro; Ando, Masahiko; Wakagi, Masatoshi
PA Japan
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002145143	A1	20021010	US 2001-940885	20010829
JP 2002305306	A2	20021018	JP 2001-106611	20010405
PRAI JP 2001-106611	A	20010405		

AB Disclosed is an active **matrix** display device using a thin film transistor as a switching element in the displaying portion or driving portion characterized in that said thin film transistor comprises an insulating substrate on which a **gate electrode**, a gate insulating film, a semiconductor layer, a **drain electrode**, a **source electrode** and a passivation film are successively laminated, and the surface portion of the semiconductor layer on the side of the passivation film is porous. The device can be stably driven with low off-current even in the case of disposing an org. passivation film and a picture element electrode on the thin film transistor.
IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(active **matrix liq. crystal** display device using thin film transistor)

L33 ANSWER 2 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:696422 HCAPLUS
DN 137:224262
TI Method of manufacture **matrix** substrate for **liquid crystal** display device
IN Yamagishi, Koichi; Kurematsu, Katsumi; Koyama, Osamu; Nakazawa, Toru
PA Japan
SO U.S. Pat. Appl. Publ., 60 pp., Division of U.S. Ser. No. 176,276.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002126233	A1	20020912	US 2002-142846	20020513
JP 11126038	A2	19990511	JP 1997-292468	19971024
JP 3199311	B2	20010820		
JP 11133892	A2	19990521	JP 1997-294467	19971027
JP 3230659	B2	20011119		
US 6512566	B1	20030128	US 1998-176276	19981021
PRAI JP 1997-292468	A	19971024		
JP 1997-294467	A	19971027		
US 1998-176276	A3	19981021		

AB A **matrix** substrate has, on a substrate, a plurality of electroconductive members to constitute **pixel electrodes** arrayed in a **matrix** pattern, and an elec. insulating member

comprising a projecting region disposed between the electroconductive members to sep. the **pixel electrodes** from each other, wherein a metal material having a higher m.p. than that of the electroconductive members is placed at the base of the projecting region. The present invention increases the mech. strength of the sepn. regions between the **pixel electrodes**, suppresses the reaction with the base layer on the occasion of thermal treatment, and increases heat resistance. The present invention also improves the dielec. withstand voltage of the capacitor film provided on the substrate and thus decreases the capacitor leak which makes redn. of cost possible.

IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method of manuf. **matrix** substrate for **liq. crystal** display)

L33 ANSWER 3 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:658519 HCAPLUS
DN 137:193969
TI Thin film transistor and active **matrix** type **liquid crystal** display device
IN Ando, Masahiko; Kawasaki, Masahiro; Wakagi, Masatoshi
PA Japan
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002117719	A1	20020829	US 2001-949846	20010912
	JP 2002252353	A2	20020906	JP 2001-49982	20010226
PRAI	JP 2001-49982	A	20010226		

AB The present invention relates in general to a thin film transistor and an active **matrix** type **liq. crystal** display device. More particularly, the invention relates to a thin film transistor which is suitable for being employed as a switching device showing the enhancement type switching characteristics, and an active **matrix** type **liq. crystal** display device employing the same. A **gate electrode**, a gate insulating layer, a semiconductor layer, a **drain electrode**, a **source electrode** and a passivation insulating layer are fabricated in turn on an insulating substrate, thereby forming a thin film transistor. The thin film transistor is designed in such a way that a Si oxide film is employed as a 2nd gate insulating layer adjacent to the semiconductor layer; a thickness of the Si oxide film is set to the range of 0.5-3.0 nm; and it shows the characteristics in which when a stress voltage which is neg. with respect to the **drain electrode** and the **source electrode** is applied to the **gate electrode**, the operating threshold voltage is reduced.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(thin film transistor and active **matrix** type **liq. crystal** display device)

L33 ANSWER 4 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:409102 HCAPLUS
DN 136:393395
TI In-plane switching **LCD** device

IN Kim, Ik-soo
PA S. Korea
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002063835	A1	20020530	US 2001-860590	20010521
PRAI KR 2000-27850	A	20000523		

AB The in-plane switching **liq. crystal** display (IPS **LCD**) according to the present invention implements a plurality of transparent common and **pixel electrodes**. Since the plurality of common and **pixel electrodes** are made from the transparent material on the same plane, the IPS **LCD** device has a high aperture ratio, a high brightness quality, and therefore a low power consumption. In another aspect, the IPS **LCD** device according to the present invention implements overlapped data line and outermost common electrode. To form the overlapped data line and outermost common electrode, an org. passivation layer is used such that cross talk between the data line and the outermost common electrode is prevented. Then, because the overlapped data line and outermost common electrode serve as a black **matrix** such that no black **matrix** is needed. Therefore, an aperture ratio of the IPS **LCD** device is further improved.
IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(second insulating layer; in-plane switching **LCD** device with high aperture ration and high brightness and low power consumption)

L33 ANSWER 5 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:403851 HCAPLUS
DN 136:394396
TI Method for fabricating polysilicon thin film transistor.
IN Yi, Jong Hoon; Lee, Sang Gul
PA LG. Philips LCD Co., Ltd., S. Korea
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6395571	B1	20020528	US 2000-665119	20000920
PRAI KR 1999-40371	A	19990920		

AB Fabrication of polysilicon thin-film transistor (TFT) having lightly doped drain or offset structure. Fabrication includes forming a semiconductor layer, a gate insulating film, and a **gate electrode** on a substrate. Then, forming lightly doped impurity regions in the semiconductor layer on both sides of the **gate electrode** . Next, forming an insulating film having a thickness that gradually becomes thinner away from the **gate electrode**. Then, forming heavily doped impurity regions in the lightly doped impurity regions in the semiconductor layer on both sides of the gate, resulting in regions with continuously varied impurity concns. The polysilicon TFT is suitable for use in active-**matrix liq. crystal** displays (**LCD**).
IT **7631-86-9D**, Silicon oxide, nonstoichiometric **12033-89-5D** , Silicon nitride, nonstoichiometric

RL: DEV (Device component use); USES (Uses)
(fabrication of polysilicon TFT suitable for use in active-**matrix LCD**)
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L33 ANSWER 6 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:172375 HCAPLUS
DN 136:207810
TI **Liquid crystal** display device and method of fabricating the same
IN Yoo, Soon-sung; Kwak, Dong-yeung; Kim, Hu-sung; Jung, Yu-ho; Kim, Yong-wan; Park, Duk-jin; Lee, Woo-chae
PA S. Korea
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002027622	A1	20020307	US 2001-919614	20011114
KR 2000-44916	A	20000802		

PI
PRAI
AB A **liq. crystal** display device and a method of fabricating the same are disclosed in the present invention. More specifically, the method includes the steps forming a gate line on the first substrate sequentially forming a first insulating layer, an amorphous silicon layer, and a metal layer on the first substrate, patterning the metal layer to form a data line, forming a second insulating layer on the data line, patterning the second insulating layer and the amorphous silicon layer to form a passivation layer and an active layer, resp., forming a **pixel electrode** at a pixel region defined by the gate and data lines, assembling the first substrate and the second substrate having a black **matrix** thereon, wherein the black **matrix** vertically overlaps at least one boundary line defined by different exposures during step-and-repeat exposure processes; and forming a **liq. crystal** layer between the first and second substrates.
IT **7631-86-9**, Silicon dioxide, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(insulating layer; fabrication method of thin film transistor array substrate for **liq. crystal** display)

L33 ANSWER 7 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:143176 HCAPLUS
DN 136:175586
TI **Liquid crystal** display device and method of fabricating the same
IN Kim, Jong-woo; Soh, Jae-moon; Ha, Young-hun
PA S. Korea
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002021403	A1	20020221	US 2001-885527	20010621
KR 2000-34298	A	20000621		

PI
PRAI

AB A high yield manufg. method of fabricating an active **matrix liq. crystal** display is described. The method includes steps of forming a first metal layer on the substrate to form a gate line including a **gate electrode**, a gate pad, and a first capacitor electrode, forming an insulating layer, an active layer, and a second metal layer on the substrate, patterning the second metal layer to form a data line including a data pad, a **source electrode**, a **drain electrode**, and a second capacitor electrode, forming a passivation layer to cover the second metal layer, forming a photoresist on the passivation layer, exposing the photoresist using a mask having a light shielding portion, a light transmissive portion, and a semi-transmissive portion, forming a first photoresist portion, a second photoresist portion, and a third photoresist portion, patterning the passivation layer, the active layer, and the insulating layer, and forming a **pixel electrode** on the passivation layer.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(insulating material; high yield manufg. method for active **matrix liq. crystal** displays)

L33 ANSWER 8 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:692073 HCAPLUS
DN 135:249550
TI Active-**matrix** substrates possessing **multilayer dielectric** underlayers for electrooptical apparatus and their fabrication
IN Ishiguro, Hideto; Takanabe, Shoichi
PA Seiko Epson Corp., Japan; Mitsubishi Electric Corp.
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001255554	A2	20010921	JP 2000-65271	20000309
PRAI	JP 2000-65271		20000309		

AB The substrates possess the outer and the inner dielec. underlayers, where n in the inner underlayers are (stepwisely) graded in the thickness direction from n0 to n1 (n0, n1 = n of the substrates and of the outer underlayers, resp.). The underlayers are manufd. by CVD using SiH4, N2O, NH3, H2, and N2 source gases while increasing flow ratio of NH3, H2, and of N2 to that of N2O. The generation of interference fringes in the underlayers can be avoided resulting in excellent colorlessness of the substrates.

IT **7631-86-9**, Silica, properties **12033-89-5**, Silicon nitride, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(diffusion barrier layers; active-**matrix** substrates possessing n-graded **multilayer dielec.** underlayers for **liq. crystal** displays)

L33 ANSWER 9 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:593248 HCAPLUS
DN 135:161035
TI Tri-layer process for forming a thin film transistor **matrix** of an **LCD** with reduced masking steps
IN Jen, Tean-Sen

PA Hannstar Display, Inc., Taiwan
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6274400	B1	20010814	US 2000-708882	20001108
TW 441133	B	20010616	TW 2000-89103433	20000225

PRAI TW 2000-89103433 A 20000225

AB A simplified tri-layer process for forming a thin film transistor **matrix** for a **liq. crystal** display is disclosed. By using a backside exposure technique twice, 2 masking steps for patterning an **etch** stopper layer, and an upper doped and a lower intrinsic semiconductor layers, resp., can be omitted. Further, owing to the back-exposing energy for patterning the semiconductor layers is less than that for patterning the **etch** stopper layer, the resulting **etch** stopper layer is enclosed with the resulting semiconductor layers, and the **contact** of the 2 semiconductor layers can be achieved.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(device insulating layer; tri-layer process for forming TFT **matrix** of **LCD** with reduced masking steps)

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L33 ANSWER 10 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:469342 HCAPLUS
DN 135:68660
TI In-plane switching mode **liquid crystal** display devices
IN Chukichi, Yoshiaki; Hirakata, Junichi; Ono, Kikuo
PA Hitachi Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 21 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001174818	A2	20010629	JP 1999-355358	19991215

PRAI JP 1999-355358 19991215

AB The devices comprise a **liq. crystal** layer sandwiched in between a 1st substrate, equipped with thin-film transistors, **pixel electrodes**, and counter electrodes, and a 2nd substrate, equipped with color filter layers sepd. by black **matrix**. In the above stated device, the 1st substrate surface, which contacts with the **liq. crystal** layer is equipped with an alignment layer, formed by inclined vapor phase deposition. The alignment layer may be Si nitride or Si oxide. Generation of after image due to degrdn. of orientation conditions of the **liq. crystals** are prevented.

IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(in-plane switching mode **liq. crystal** display devices equipped with alignment layers formed by inclined vapor phase deposition)

L33 ANSWER 11 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:336571 HCAPLUS
DN 134:334359
TI Active **matrix** substrate with passivation layer and its manufacture
IN Ibita, Satoshi; Yamaguchi, Hirotaka; Tanaka, Hiroaki; Hayase, Takasuke; Kano, Hiroshi; Kaneko, Wakahiko; Miyahara, Tae; Sakamoto, Michiaki; Nakata, Shinichi
PA NEC Corp., Japan; NEC Kagoshima, Ltd.
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001125134	A2	20010511	JP 1999-304682	19991026
PRAI	JP 1999-304682		19991026		

AB The active **matrix** substrate is manufd. by the steps of (1) forming a transparent electrode and a metal layer on a transparent insulating substrate, and forming **gate electrodes**, gate lines, and **pixel electrodes** using 1st mask, (2) forming a gate insulating layer and an amorphous Si semiconductor layer on the **gate electrode** and processing the gate insulating layer and amorphous Si layer to desired shape using 2nd mask, (3) forming a passivation layer covering the surface and the side of the amorphous Si layer and forming an opening through the passivation layer for contacting the **source/drain electrodes** with the Si layer on the Si layer using 3rd mask and forming another opening through the passivation layer and metal layer for exposing the metal oxide layer on the **pixel electrode**, and (4) forming an electrode layer on the passivation layer and the upperside of the opening and forming lines connecting the exposed Si layer and the **pixel electrode** and **drain** lines using 4th mask. The obtained active **matrix** substrate is also claimed. Channel protective type active **matrix** substrate in which amorphous Si layer is covered with the passivation layer is obtained easily.
IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(passivation layer; manuf. of channel protective-type active **matrix** substrate having passivation layer for **liq. crystal** display)

L33 ANSWER 12 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:225551 HCAPLUS
DN 134:259295
TI Thin film transistor **liquid crystal** display panel without black **matrix**
IN Hamada, Hiroki; Ide, Daisuke
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001083895	A2	20010330	JP 1999-263502	19990917
PRAI	JP 1999-263502		19990917		

AB The invention relates to the TFT **liq. crystal** display in which a **dielec. multilayer** film is used instead of the conventional black **matrix**. The **dielec. multilayer** film includes a high refractive layer made up of Si and a low refractive layer made up of Si oxide. The display shows improved high contrast. The use of the **dielec. multilayer** film instead of the conventional black **matrix** reduced the **liq. crystal** display prodn. cost.

IT **7631-86-9**, Silicon oxide, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(low refractive layer in **dielec. multilayer** film of TFT **liq. crystal** display panel)

L33 ANSWER 13 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:222043 HCAPLUS
DN 134:259281
TI Thin film transistor suitable for use in an active **matrix** type display and method of fabricating the same
IN Jinno, Yushi; Wakita, Ken; Minegishi, Masahiro
PA Sanyo Electric Co., Ltd., Japan; Sony Corporation
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6207971	B1	20010327	US 1997-997763	19971224
	JP 10189990	A2	19980721	JP 1996-350619	19961227
	US 2001005020	A1	20010628	US 2001-753397	20010103
PRAI	JP 1996-350619	A	19961227		
	US 1997-997763	A3	19971224		

AB Active **matrix** type display app. which comprises a plurality of pixels and a plurality of drive elements, each drive element including a thin film transistor of a bottom gate structure, the thin film transistor having: an insulator substrate; a **gate electrode** located on the insulator substrate; an insulator film provided on the insulator substrate and the **gate electrode**; and a polycryst. silicon film located on the insulator film, a channel defined in a first portion of the polycryst. silicon film over the **gate electrode**, and a **drain** and a source defined in second and third portions of the polycryst. silicon film over the insulator substrate, is described in which the grain sizes of the drain and the source are greater than a grain size of the channel by laser annealing.

IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(active **matrix** type displays using thin-film transistors with drainss and sources with large grains)

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L33 ANSWER 14 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:69412 HCAPLUS
DN 134:140364
TI Manufacture of thin-film transistor and electrooptic device
IN Onizuka, Tatsuya
PA Seiko Epson Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001028439	A2	20010130	JP 1999-200876	19990714
PRAI JP 1999-200876		19990714		

AB The invention relates to a process for making a thin-film transistor for use in an electrooptical imaging device, e.g. an active **matrix liq. crystal** display device, wherein the process includes forming a protecting film, e.g. SiO2 or SiN film, on a **gate electrode**, e.g. Al/TiN **gate electrode**, prior to forming a resist mask film for ion implantation process, thereby preventing damage of the **gate electrode**.

IT **7631-86-9**, Silicon oxide, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**gate electrode**-protecting film; manuf. of thin-film transistor for electrooptic device)

L33 ANSWER 15 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:62455 HCAPLUS
DN 134:124647
TI Dry etching method for forming tungsten and tungsten compound wiring of arbitrary taper angle in a semiconductor device
IN Suzawa, Hideomi; Ono, Koji
PA SEL Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 32 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1071124	A2	20010124	EP 2000-115333	20000714
EP 1071124	A3	20011024		
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
JP 2001035808	A2	20010209	JP 1999-206954	19990722
CN 1282107	A	20010131	CN 2000-121738	20000724
PRAI JP 1999-206954	A	19990722		

AB A dry etching method for forming W wiring having a tapered shape and having a large specific selectivity with respect to a base film is provided. If the bias power d. is suitably regulated, and if desired portions of a W thin film are removed using an etching gas having F as its main constituent, then the W wiring having a desired taper angle can be formed. The W and tungsten compd. wirings are gate wirings of thin film transistor. The semiconductor devices are active **matrix liq. crystal** display devices, EL display devices, and electronic appliances.

IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(insulating films; dry etching method for forming tungsten and tungsten compd. wiring of arbitrary taper angle in a semiconductor device)

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(quartz, thin film transistor substrate, insulating film; dry etching method for forming tungsten and tungsten compd. wiring of arbitrary

taper angle in a semiconductor device)

L33 ANSWER 16 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:46374 HCAPLUS
DN 134:124597
TI Production method of thin film transistor, production method of active-**matrix** substrate and production method of electro-optic device.
IN Kobashi, Hiroshi
PA Seiko Epson Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001015760	A2	20010119	JP 1999-186651	19990630
PRAI JP 1999-186651		19990630		

AB Methods for fabricating thin-film transistors are described which entail forming a semiconductor channel layer on a substrate; covering the semiconductor layer with a first insulating layer; forming an aluminum-contg. **gate electrode** on the first insulating layer; and covering the **gate electrode** layer with a second insulating layer, with the temp. during processing of the second insulating layer being in the range 200-450.degree.. Methods for producing active **matrix** structures entailing the prodn. of multiple transistors on a substrate are also described. Electrooptical devices (e.g., **liq. crystal** displays) employing the active **matrix** substrates are described.
IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(thin film transistor and active-**matrix** substrate prodn. and electrooptical devices using them)

L33 ANSWER 17 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:687023 HCAPLUS
DN 133:289782
TI Semiconductor devices for TFTs, fabrication thereof, and active-**matrix liquid crystal** display devices
IN Ishihara, Shingo; Wakaki, Masatoshi; Ando, Masahiko
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000269504	A2	20000929	JP 1999-69529	19990316
TW 473639	B	20020121	TW 2000-89103612	20000301
US 6300988	B1	20011009	US 2000-526557	20000316
US 2002012080	A1	20020131	US 2001-949091	20010910
PRAI JP 1999-69529	A	19990316		
US 2000-526557	A1	20000316		

AB The title fabrication involves (1) forming on a glass substrate with a **gate electrode**, a gate insulator film, and **source/drain electrodes**, (2) patterning an insulator film over the surface to expose the **gate electrode**, and (3) depositing an org. semiconductor film to give a

channel region for insulator-removed area as a same size to the **gate electrode**. The process gives the semiconductor device channel optimization for decrease of drain OFF current and for prevention of write in the **liq.-crystal** pixels by adjacent signal wiring.

IT **7631-86-9P**, Silica, properties
RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); USES (Uses)
(gate insulator film; semiconductor devices for TFTs, fabrication thereof, and active-**matrix liq. crystal** display devices)

IT **12033-89-5P**, Silicon nitride, properties
RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); USES (Uses)
(semiconductor devices for TFTs, fabrication thereof, and active-**matrix liq. crystal** display devices)

L33 ANSWER 18 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:686695 HCAPLUS
DN 133:288951
TI Fabrication of a thin-film transistor array substrate for an active-**matrix liquid-crystal** display
IN Kashimoto, Miyuki; Kubo, Akira; Nakajima, Madoka; Imamura, Yasuyuki
PA Toshiba Corp., Japan; Toshiba Electronic Engineering Corp.
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000267595	A2	20000929	JP 1999-68034	19990315
PRAI	JP 1999-68034		19990315		

AB The invention relates to a process for making a thin-film transistor (TFT) array substrate for an active-**matrix liq.-crystal** display (**LCD**), wherein the **contact holes** are formed by a combination of wet and dry **etching** process.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of thin-film transistor array substrate for active-**matrix liq.-crystal** display)

L33 ANSWER 19 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:227993 HCAPLUS
DN 132:229575
TI **Matrix** substrate for **liquid-crystal** display device
IN Miyawaki, Mamoru; Kurematsu, Katsumi; Koyama, Osamu; Fukumoto, Yoshihiko; Nakazawa, Toru
PA Canon K. K., Japan
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 61 pp.
CODEN: CNXXEV
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	CN 1184954	A	19980617	CN 1997-122897	19971017

	JP 10177181	A2	19980630	JP 1997-279014	19971013
	JP 3249077	B2	20020121		
	EP 837355	A2	19980422	EP 1997-308261	19971017
	EP 837355	A3	19990210		
	EP 837355	B1	20020904		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6157429	A	20001205	US 1997-953730	19971017
PRAI	JP 1996-276532	A	19961018		
	JP 1997-279014	A	19971013		

AB A **matrix** substrate for a **liq.-crystal** display device comprises a **matrix** of **pixel electrodes**, a driving circuit for supplying elec. signals to the **pixel electrodes**, and a sealing layer, wherein an insulating layer is formed in the areas between the **pixel electrodes** in order to form a continuous even surface over the **pixel electrodes**, and a light-shielding layer is placed under the **pixel electrodes**. The **pixel electrodes** are made of Al, Ti, Ta, W, Cr, Au, or Ag, and the insulating layer is made of SiO2, Si3N4, or Ta2O5.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(**liq.-crystal** display device **matrix** substrates contg. insulating layers of)

L33 ANSWER 20 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:113144 HCAPLUS
DN 132:159003
TI Active **matrix** substrate with removal of portion of insulating film overlapping source line and **pixel electrode** and method for producing the same
IN Kawai, Katsuhiro; Yamakawa, Shinya; Okamoto, Masaya; Katayama, Mikio
PA Sharp Kabushiki Kaisha, Japan
SO U.S., 23 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6025892	A	20000215	US 1997-839268	19970417
	JP 10010583	A2	19980116	JP 1997-53085	19970307
	TW 448332	B	20010801	TW 1997-86105157	19970421
PRAI	JP 1996-100074	A	19960422		
	JP 1997-53085	A	19970307		

AB Fabrication method for an active **matrix** substrate for **liq. crystal** displays is described. The method produces the active **matrix** free from structural defects and includes the following steps: (1) forming the plurality of the parallel first lines on the substrate (gate lines), (2) forming an insulating film on the entire substrate surface covering the first lines, (3) removing the portions of the insulating film, (4) forming the second lines (source lines), (5) forming **source** and **drain electrodes** of the switching elements, and (6) forming the **pixel electrodes** in such way that the gaps are provided between them and the second lines. The switching elements are thin film transistors including **gate electrodes**, **source electrodes**, **drain electrodes** and semiconductor portions.

IT **12033-89-5**, Silicon nitride, processes

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(gate insulating film; fabrication of structural defect free active **matrix** substrate for **liq. crystal** displays)
IT **7631-86-9**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(interlayer insulating film; fabrication of structural defect free active **matrix** substrate for **liq. crystal** displays)
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L33 ANSWER 21 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:34494 HCAPLUS
DN 132:86699
TI Thin-film transistor panel for **liquid-crystal** display
IN Yamashita, Yasuhiko; Ishida, Satoshi; Masuno, Toru
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000012863	A2	20000114	JP 1998-172974	19980619
PRAI	JP 1998-172974		19980619		

AB The invention relates to a thin-film transistor panel, suited for use as a driver for active-**matrix liq.-crystal** displays and electroluminescent displays, wherein the side-**etching** and overetching of **contact holes** is suppressed.
IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(thin-film transistor panel for **liq.-crystal** display)

L33 ANSWER 22 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:388380 HCAPLUS
DN 131:26640
TI Electronic devices containing thin-film transistors
IN Deane, Steven Charles; Shannon, John Martin
PA Koninklijke Philips Electronics N.V., Neth.; Philips AB
SO PCT Int. Appl., 20 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9930369	A2	19990617	WO 1998-IB1815	19981113
	WO 9930369	A3	19990826		
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 974164	A2	20000126	EP 1998-951630	19981113
	R: DE, FR, GB				
	JP 2001511317	T2	20010807	JP 1999-530417	19981113
	US 6064091	A	20000516	US 1998-209085	19981210
PRAI	GB 1997-26094	A	19971210		

WO 1998-IB1815 W 19981113

AB A thin-film transistor in an electronic device such as an active **matrix liq.-crystal** display panel having an intrinsic amorphous Si semiconductor layer providing a channel region between **source** and **drain electrodes** includes directly adjacent to the side of the semiconductor layer remote from the **gate electrode** at the channel region a layer of amorphous semiconductor material which has a high defect d. and low cond. that serves to provide recombination centers for photogenerated carriers. Leakage problems due to the photoconductive properties of the intrinsic semiconductor material are then reduced. Conveniently, a hydrogenated Si-rich amorphous Si-contg. material (oxide, nitride, etc.) can be used for the recombination center layer.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride (Si3N4), uses
RL: DEV (Device component use); USES (Uses)
(thin-film transistors having hydrogenated amorphous recombination center layers of)

L33 ANSWER 23 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:356357 HCAPLUS
DN 131:177289
TI Normally white reflective twisted nematic mode for silicon-chip-based light valves
AU Hirota, Shoichi; Tsumura, Makoto; Nakagawa, Hideki; Miyazawa, Toshio; Takemoto, Iwao
CS Hitachi Research Lab, Hitachi, Ltd., Hitachi-shi Ibaraki-ken, Japan
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3635(Liquid Crystal Materials, Devices, and Applications VII), 86-94
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB Cryst. silicon-chip-based reflective light valves are suitable for realizing high definition and bright **liq. crystal** projectors. We have developed an XGA silicon-chip-based light valve with a diagonal display area of 1 in. A normally white reflective twisted nematic mode is selected for the valve. An optimum condition of the mode is anal. solved by the Jones **matrix** method. This mode is suitable for a narrow cell gap and a fast response time can be expected. This mode also has a stable contrast ratio even with temp. and/or cell gap fluctuation. In addn., the driving voltage of this mode is low and it has good chromaticity with small retardation. The cell gap of the light valve is 2 .mu.m. The cell gap support is made using spacer posts formed on the silicon chip with a photo-definable resin. The response time is 12 ms including both rise and fall times. The contrast ratio is more than 400 at 5 Vrms.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(mirror MOS chip of XGA silicon-chip-based light valve)

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L33 ANSWER 24 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:119956 HCAPLUS
DN 130:147510
TI Fabrication of **contact holes** in a thin-film transistor active-**matrix** substrate for a **liquid-crystal** display

IN Ura, Masashi; Takanabe, Shoichi; Nakamura, Nobuhiro; Endo, Yukio; Ito, Osamu
PA Mitsubishi Electric Corp., Japan; Kabushiki Kaisha Advanced Display
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11045879	A2	19990216	JP 1998-128011	19980512
	US 6054392	A	20000425	US 1997-984064	19971203
PRAI	JP 1997-137255		19970527		

AB The invention relates to a process for making a **contact hole** in a thin-film transistor (TFT) active-**matrix** substrate for a **liq.-crystal** display (**LCD**), wherein the **contact hole** is formed by dry-**etching** a Si nitride insulator film on a Cr film.
IT **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of **contact holes** in a thin-film transistor active-**matrix** substrate for a **liq.-crystal** display)
IT **7631-86-9**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(vacuum; fabrication of **contact holes** in a thin-film transistor active-**matrix** substrate for a **liq.-crystal** display)

L33 ANSWER 25 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:599470 HCAPLUS
DN 129:267993
TI Active **matrix liquid crystal** display
IN Shimada, Shinji
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10239698	A2	19980911	JP 1997-40487	19970225
	US 5905548	A	19990518	US 1998-6267	19980113
PRAI	JP 1997-40487		19970225		

AB The title display includes an org. insulator layer (.ltoreq.3.5 dielec. const.) formed on a bus lines, and an inorg. insulator layer (.gtoreq.3.5 dielec. const.) formed on **pixel electrodes**. The org. insulator layer may be made of polyimide, and the inorg. insulator layer may be made of Si oxide or Si nitride.
IT **7631-86-9**, Silicon oxide, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in insulator layer of active **matrix liq. crystal** display)

L33 ANSWER 26 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:334246 HCAPLUS

DN 129:61652
TI Thin-film transistor and fabrication thereof
IN Hirose, Takashi; Tsuboi, Nobuyuki; Tamura, Tatsuhiko
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10135465	A2	19980522	JP 1996-286592	19961029
	JP 3182351	B2	20010703		
PRAI	JP 1996-286592		19961029		

AB The invention relates to a TFT (thin film transistor) substrate, suited for use as a switching device in active-**matrix LCD** (**liq.-crystal** display) panels, wherein the Mo contact surface between the **source-drain electrodes** and the ITO **pixel electrodes** minimizes the resistance.
IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(thin-film transistor for **liq.-crystal** display)

L33 ANSWER 27 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:186466 HCAPLUS
DN 128:238116
TI Fabricating a thin-film transistor **matrix** device
IN Oki, Ken-ichi; Yanai, Ken-ichi; Wada, Tamotsu; Ohgata, Koji; Takizawa, Yutaka; Okabe, Masahiro; Tanaka, Tsutomu
PA Fujitsu Ltd., Japan
SO U.S., 88 pp., Division of U. S. Ser. No. 134,824, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5728592	A	19980317	US 1995-499000	19950706
	JP 06194688	A2	19940715	JP 1993-221645	19930907
	US 5994173	A	19991130	US 1997-941224	19970926
PRAI	JP 1992-271630	A	19921009		
	JP 1993-168807	A	19930708		
	JP 1993-221645	A	19930907		
	US 1993-134824	B3	19931012		
	US 1995-499000	A3	19950706		

AB A thin-film transistor **matrix** device, esp. for active-**matrix liq.-crystal** displays, is fabricated by forming a transparent conductor film and a metal film on an insulating substrate in this order. The metal and transparent conductor films are patterned together to form **pixel electrodes** and **drain** or gate bus lines. **Source** and **drain electrodes** may also be formed from the transparent conductor and metal films. A semiconductor layer, an insulating film, and a conductor film may be formed on the entire surface in this order. In this case, the conductor film, the insulator film, and the semiconductor layer are patterned to form an active layer from the semiconductor layer, gate insulating films from the insulating film, and **gate electrodes** and gate bus lines from the conductor film. By patterning the conductor film, the insulating film, and the semiconductor layer, the metal film of the **pixel electrodes** and

drain bus lines is exposed. Alternatively, the metal film may be patterned with the semiconductor layer, insulating film, and conductor film to expose the transparent conductor film. A current is applied to the drain or gate bus lines in an electrolyte soln. to selectively form a film on the drain or gate bus lines. The film may be a protective film serving as a mask to allow the metal film on the **pixel electrodes** to be etched.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating a thin-film transistor **matrix** device contg.)

L33 ANSWER 28 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:154522 HCAPLUS
DN 128:264006
TI Normally white-mode reflecting **liquid crystal** display with increased image contrast
IN Ookubo, Tatsuya; Hirota, Shoichi; Abe, Makoto
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10062797	A2	19980306	JP 1996-217067	19960819
PRAI JP 1996-217067		19960819		

AB The title **liq. crystal** display comprises a **liq. crystal** layer sandwiched between an active **matrix** substrate having an active element for each **pixel electrode** and a counter electrode having a transparent electrode, wherein a Si oxide or Si nitride thin film with the tapered edges is formed under the edge of the **pixel electrode**. The **pixel electrodes** were able to reduce lateral field therebetween.

IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(normally white-mode reflecting **liq. crystal** display with increased image contrast)

L33 ANSWER 29 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:717610 HCAPLUS
DN 127:365044
TI Fabrication of thin-film transistor for **liquid-crystal** display
IN Ishio, Noriaki
PA Advanced Display K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09283492	A2	19971031	JP 1996-90937	19960412
PRAI JP 1996-90937		19960412		

AB The invention relates to a process for making a thin-film transistor, suited for use as a driver for active-**matrix liq.**-

crystal displays, wherein the angle of taper for the **etching** the edge of the gate **contact** layer is precisely controlled by the use of monitor patterns.
IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(taper **etching** in fabrication of thin-film transistor for **liq.-crystal** display)

L33 ANSWER 30 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:636468 HCAPLUS
DN 127:325314
TI Thin-film semiconductor active-**matrix** array for **liquid -crystal** display and fabrication thereof
IN Furuta, Mamoru
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09252136	A2	19970922	JP 1996-58918	19960315
PRAI	JP 1996-58918		19960315		

AB The invention relates to a semiconductor TFT active-**matrix** array, suited for use in **liq.-crystal** displays, wherein the **multilayer**-structure gate **insulator** film provide redundancy in protection against pinholes.
IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor TFT active-**matrix** array for **liq.-crystal** display)

L33 ANSWER 31 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:614019 HCAPLUS
DN 127:286001
TI **Liquid crystal** display with improved contrast
IN Terumoto, Koji
PA Rohm Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09230348	A2	19970905	JP 1996-39660	19960227
PRAI	JP 1996-39660		19960227		

AB An orientation film is formed only on the **pixel electrodes** of the **liq. crystal** display to improve high contrast. The orientation film is formed by (1) printing the orientation film only on the **pixel electrodes** and rubbing the orientation film, (2) printing the orientation film on the **pixel electrode**-bearing substrate and rubbing only the orientation film located on the **pixel electrodes**, (3) printing the orientation film on the **pixel electrode** -bearing substrate and photolithog. patterning the orientation film via the photomask, or (4) printing the orientation film on the **pixel**

electrode-bearing substrate and coating the orientation film not on the **pixel electrodes** with inorg. insulators. The display improves its contrast without using a black **matrix**.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(orientation film coated with)

L33 ANSWER 32 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:574600 HCAPLUS
DN 127:242022
TI Fabrication of thin-film transistor (TFT) having reliable **contact**
IN Cho, Koyu
PA Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09213968	A2	19970815	JP 1996-332894	19961127
	US 5940732	A	19990817	US 1996-753428	19961125
PRAI	JP 1995-332629		19951127		

AB The invention relates to a process for making a semiconductor device, esp., a TFT, having an anodizable metal **gate electrode**, suited for use in a active **matrix liq. crystal** display, wherein the TFT contains **multilayered** interlayer **insulating** films having specified **etching** rates, for forming a tapered **contact hole**, thereby improving reliability of the **contact**.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of TFT having reliable **contact**)

L33 ANSWER 33 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:508359 HCAPLUS
DN 127:197798
TI Active **matrix** substrate for **liquid crystal** device
IN Jinnai, Norihide; Dojiro, Masayuki; Shibusawa, Makoto; Kamata, Yoshitaka
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09197436	A2	19970731	JP 1996-8989	19960123
PRAI	JP 1996-8989		19960123		

AB An aluminum **gate electrode** and gate wiring are formed on a substrate by photolithog. below 130.degree., and a 1st gate insulating film made from a high hardness .alpha.-silicon oxide is formed by plasma CVD below 150.degree.. The substrate can be manufd. at a low cost manuf. without using high m.p. metals and without causing Al hillock.

IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: TEM (Technical or engineered material use); USES (Uses)

(used for gate insulating film in active **matrix** substrate for **liq. crystal** device)

L33 ANSWER 34 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:341850 HCAPLUS
DN 126:324273
TI Semiconductor or **liquid-crystal** device, an active-**matrix** substrate, and their production
IN Fukumoto, Yoshihiko
PA Canon K. K., Japan
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 768710	A2	19970416	EP 1996-306683	19960913
	EP 768710	A3	19970730		
	R: DE, FR, GB, IT, NL				
	JP 09148329	A2	19970606	JP 1996-241939	19960912
	TW 469420	B	20011221	TW 1996-85111218	19960913
PRAI	JP 1995-236865	A	19950914		
	JP 1996-241939	A	19960912		

AB The prodn. of a semiconductor device comprises polishing a region of an elec. conductive material serving as an electrode or a wiring line in an insulating layer formed on a semiconductor region, the region of elec. conductive material being elec. connected to the semiconductor region, where a region of another material is formed within the elec. conductive material to be polished. The prodn. of an active-**matrix** substrate comprises polishing metal **pixel electrodes** provided at intersections of multiple signal lines and multiple scanning lines and a means for applying voltage to the pixels, where a region of another material is formed within the **pixel electrode** to be polished.
IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(prodn. of semiconductor devices and **liq.-crystal** devices and active-**matrix** substrates contg.)

L33 ANSWER 35 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:216077 HCAPLUS
DN 126:271074
TI Method for manufacturing a thin-film transistor
IN Ha, Yong M.
PA LG Electronics Inc., S. Korea
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5612234	A	19970318	US 1995-539156	19951004
	US 5767530	A	19980616	US 1997-938318	19970926
PRAI	US 1995-539156		19951004		
	US 1996-758564		19961203		

AB A thin-film transistor for incorporation into an active-**matrix** **liq.-crystal** display includes an active layer provided

on a substrate. An electrode insulating layer is formed on the active layer, and a **gate electrode** including 1st and 2nd gate layers is provided on the electrode insulating layer. The 2nd gate layer overlies the 1st gate layer and has a width greater than the 1st gate layer. LDD regions self-aligned with the 2nd gate layer are provided in the active layer adjacent to the source and drain regions. The active layer further includes a channel region located under the 1st gate layer and offset regions located under portions of the 2nd gate layer extending beyond the 1st gate layer on opposite sides of the channel region. In the manuf. of the thin-film transistor, an active layer is formed on a substrate; an electrode insulating layer is formed on the active layer; an oxidizable 1st **gate electrode** and a nonoxidizable 2nd **gate electrode** of the same widths are stacked on the electrode insulating layer; low-concn. impurity ions are implanted in the active layer using the 2nd **gate electrode** as a mask; the sides of the 1st electrode are oxidized to form oxide layers that reduce the width of the 1st **gate electrode**; and high-concn. impurity ions are implanted, using the 2nd **gate electrode** and the oxide layers as implantation masks.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manuf. of thin-film transistors contg.)

L33 ANSWER 36 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:728292 HCAPLUS
DN 126:41518
TI Manufacture of semiconductor integrated circuit
IN Cho, Koju
PA Handotai Energy Kenkyusho, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08255875	A2	19961001	JP 1996-23271	19960117
	JP 3270674	B2	20020402		
	US 5814529	A	19980929	US 1996-585916	19960116
	JP 11097714	A2	19990409	JP 1998-216904	19960117
	US 6320224	B1	20011120	US 1998-110895	19980707
	US 2002055206	A1	20020509	US 2001-987607	20011115
PRAI	JP 1995-22256	A	19950117		
	US 1996-585916	A3	19960116		
	JP 1996-23271	A3	19960117		
	US 1998-110895	A3	19980707		

AB The manuf. involves the following steps; (1) forming a interlayer insulating substance composed of .gtoreq.2 layers having different dry **etching** property, (2) **etching** the upper insulating layer using the lower insulating layer as an **etching** stopper, and using a 1st mask, (3) selectively **etching** the partially exposed lower insulating layer using a 2nd mask, and (4) forming a circuit comprising a **contact hole** (formed by the **etching** of the upper- and lower insulating layers), and a capacitor (a part where only the upper insulating layer is **etched** and removed). The upper- and lower insulating layers may be Si nitride, and Si oxide, resp. The manuf. enables forming a small elec. capacitor with large capacity, and is suited for manuf. of active **matrix** -type semiconductor app., esp. **liq. crystal** display

devices.
IT **7631-86-9**, Silicon dioxide, uses **12033-89-5**, Silicon nitride (si3n4), uses
RL: DEV (Device component use); USES (Uses)
(insulator in capacitor; in manuf. of semiconductor integrated circuit having capacitor)

L33 ANSWER 37 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:686824 HCAPLUS
DN 125:343063
TI Manufacture of thin film device having insulating film
IN Matsumura, Mitsuyoshi
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08241892	A2	19960917	JP 1995-66689	19950302
PRAI	JP 1995-66689		19950302		

AB The manuf. involves the following steps; (1) forming an insulating film formed by CVD or sputtering, and a passivation film contg. a Si oxide film (at interlayers of the insulating film) at formed by coating, on Al or Al alloy, and (2) forming a semiconductor- or wiring layer on the passivation film. The device is hillock free, and the manuf. is suited for active **matrix**-type **liq. crystal** display device installed with a thin-film transistor.
IT **12033-89-5**, Silicon nitride (si3n4), uses
RL: DEV (Device component use); USES (Uses)
(passivation film component; manuf. of thin film transistor for **liq. crystal** display device)
IT **7631-86-9P**, Silicon dioxide, preparation
RL: DEV (Device component use); IMF (Industrial manufacture); PREP (Preparation); USES (Uses)
(passivation film component; manuf. of thin film transistor for **liq. crystal** display device)

L33 ANSWER 38 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:483183 HCAPLUS
DN 125:128021
TI **Liquid-crystal** display device and its manufacture
IN Ishiguro, Kenichi
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08122813	A2	19960517	JP 1994-253883	19941019
	JP 3105408	B2	20001030		
	US 5899548	A	19990504	US 1995-542942	19951013
PRAI	JP 1994-253883	A	19941019		

AB In the active **matrix**-type **liq.-crystal** display device, contg. a thin-film transistor and a storage capacitor, the capacitor comprises a 1st insulating film of non-single crystal Si oxide and a 2nd insulating film of the same material with that of a gate-insulating film of the transistor, between a 1st electrode of

non-single crystal Si and a 2nd electrode. The non-single cryst. Si may be formed by implantation of polycryst. Si of .gtoreq.5 cm2/V-s field-effect electron mobility. The device is manufd. by the steps of forming a non-single cryst. Si thin film on a substrate, masking the region other than the capacitor-forming region, and oxidizing the exposed part to form an oxide film. The masking material may be a photosensitive resin compn. The device shows improved reliability of the storage capacity and prevents defect generation derived from pin holes.

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(gate-insulating film; manuf. of active **matrix**-type **liq.-crystal** display device)

IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(interlayer-insulating film; manuf. of active **matrix**-type **liq.-crystal** display device)

L33 ANSWER 39 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:464173 HCAPLUS
DN 125:102610
TI Thin film semiconductor device and active **matrix**-type **liquid crystal** display device
IN Ino, Masumitsu; Urazono, Takenobu
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08116066	A2	19960507	JP 1994-274601	19941012
PRAI JP 1994-274601		19941012		

AB The title device concerns a TFT (thin film transistor) having (1) an active layer of a semiconductor film in which a channel region is formed, (2) a **gate electrode** of a metal film, and (3) a gate insulator film between the active layer and the **gate electrode**. A Si3N4 film lies in the gate insulator film, which is a getter catching the impurity contained in the **gate electrode**. The gate insulator film may consist of a SiO2 film/a Si3N4 film/a SiO2 film, for instance. The **gate electrode** may be 0.5-1.0 % Si-contg. Al. The display device using the TFT is also claimed.

IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(gettering layer; thin film semiconductor device and active **matrix**-type **liq. crystal** display device)

IT **7631-86-9**, Silicon dioxide, uses
RL: DEV (Device component use); USES (Uses)
(thin film semiconductor device and active **matrix**-type **liq. crystal** display device)

L33 ANSWER 40 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:393767 HCAPLUS
DN 125:45330
TI Manufacture of thin-film semiconductor apparatus
IN Suzuki, Nobuaki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08097432	A2	19960412	JP 1994-254436	19940922
PRAI	JP 1994-254436		19940922		

AB The manuf. involves the steps of (1) forming a FET on a substrate using a polycryst. semiconductor thin film as an active layer, (2) forming a nondensified 1st insulating film on the transistor, (3) forming a densified 2nd insulating film, (4) implanting H ions in the 1st insulating film through the 2nd insulating film, and (5) heating the substrate to accelerate lower diffusion of H by inhibiting upper diffusion of H in the presence of the 2nd insulating film to introduce H into the active layer of the transistor. Manuf. of an active **matrix**-type **liq**.-**crystal** display device involves the steps (1), (2), (3), (4), (5), (6) foring a **pixel electrode** by connecting with the transistor, (7) bonding an another substrate (having a counter electrode) with the substrate, and (8) filling a **liq**. **crystal** between the gap. The method improves hydrogenation efficiency of the polycryst. semiconductor thin films (becoming an active layer of the thin film transistor) and inhibits damaging of the active layer.

IT **7631-86-9**, Silicon dioxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(insulating film; manuf. of active **matrix**-type **liq**.-**crystal** display device)

L33 ANSWER 41 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:197200 HCAPLUS
DN 124:248053
TI Thin film transistor, its manufacture, and **liquid** **crystal** display device using it
IN Asaba, Tetsuro
PA Canon Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08018064	A2	19960119	JP 1995-115320	19950418
PRAI	JP 1994-109100		19940426		

AB In the field-effect thin film transistor (TFT), successively comprising a transparent substrate, a **gate electrode**, a gate-insulating layer, and a semiconductor layer contg. a channel, a source, and a drain regions, the **gate electrode** comprises Si - metal silicide bilayer, and the gate-insulating film of which the part contacting with the channel consists of SiO2 . The **gate electrode** layer may be a triple layer of Si - metal silicide - Si. The metal silicide layer may be W silicide. Optionally, the semiconductor layer may be coated with a 2nd **gate** **electrode** of Si layer, via a 2nd gate-insulating film of which the part contacting with the channel being SiO2 . The manuf. comprises these steps; forming the **gate electrode** on the substrate, oxidizing (and optionally annealing) the surface, depositing the semiconductor layer to form the channel, the source, and the drain regions. The **liq**. **crystal** display device includes the TFT as a switching device of active **matrix**-type substrate. The TFT has a good light-blocking property of the multilayer **gate**

electrode, and provides improved switching characteristics with the **liq. crystal** display device.

IT **7631-86-9**, Silicon dioxide, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(gate-insulating film; manuf. of TFT and active **matrix**-type **liq. crystal** display device)

IT **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(transparent substrate; manuf. of TFT and active **matrix**-type **liq. crystal** display device)

L33 ANSWER 42 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:1006991 HCAPLUS
DN 124:133109
TI Manufacture of thin film transistor useful for **liquid crystal** display device
IN Shimomaki, Shinichi
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07273342	A2	19951020	JP 1994-83593	19940331
	JP 3358284	B2	20021216		
PRAI	JP 1994-83593		19940331		

AB A thin film transistor is manufd. by (1) successively forming a **gate electrode**, a gate-insulator, semiconductor (A), the 1st elec. insulator (B), and the 2nd insulator (C) with a different compn. from that of B, (2) dry **etching** C assocd. with protecting A by B, (3) diffusing an impurity in A through C as mask, (4) patterning A, (5) forming elec. insulating protecting layer on A, and (6) forming **contact hole**, and (7) forming **source** and **drain electrodes** contacting to **source** and drain regions on A through the **contact hole**. Alternatively, the process includes forming photoresist patterned in self-alignment and patterning of C through the resist by etchants of different **etching** rate. The process is useful for manuf. of active **matrix** liq.-cryst. display device.

IT **7631-86-9**, Silicon oxide, processes **12033-89-5**, Silicon nitride, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(elec. insulator; manuf. of thin film transistor including dry **etching** of insulator for active **matrix** device in **liq.-crystal** display device)

L33 ANSWER 43 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:999647 HCAPLUS
DN 124:43287
TI Thin-film transistor for **liquid-crystal** display
IN Oono, Eizo
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07263703	A2	19951013	JP 1994-49155	19940318
PRAI	JP 1994-49155		19940318		

AB A poly-Si thin-film transistor, suited for use as a driver for active-**matrix liq.-crystal** displays, comprises a channel region, flanked by a source and a drain, formed under the **gate electrode**, and connected to a lead contact.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(polysilicon thin-film transistor for **liq.-crystal** display)

L33 ANSWER 44 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:969756 HCAPLUS
DN 123:356843
TI Thin-film transistor for **liquid-crystal** display
IN Uchikoga, Shuichi; Ikeda, Takami; Akyama, Masahiko
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07254710	A2	19951003	JP 1994-42965	19940315
PRAI	JP 1994-42965		19940315		

AB A reverse-staggered thin-film transistor, suited for use as a driver for active-**matrix liq.-crystal** displays and image sensors, wherein the channel layer is .ltoreq.48nm thick, and the **source-drain electrode** and the **gate electrode** have an overlapping area.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(reverse-staggered thin-film transistor for **liq.-crystal** display)

L33 ANSWER 45 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:602478 HCAPLUS
DN 123:44518
TI Active **matrix liquid crystal** display device
IN Kobayashi, Kazuhiro; Murai, Hiroyuki; Hayama, Masahiro
PA Mitsubishi Denki Kabushiki Kaisha, Japan
SO U.S., 9 pp. Cont.-in-part of U.S. Ser. No. 904,272, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5414278	A	19950509	US 1994-231774	19940425
	JP 05011271	A2	19930119	JP 1991-164140	19910704
	JP 2864794	B2	19990308		
PRAI	JP 1991-164140		19910704		
	US 1992-904272		19920625		

AB A **pixel electrode** and a line for a storage capacitor are sandwiched by 1st and 2nd protecting films so as to position them in a different plane from a **gate electrode** and

source/drain lines. An insulating film for a storage capacitor and the 2nd protecting film remain at a crossing of the source line and a gate line, but part of them on a TFT is removed, when a pattern of the removal is at least partially deviated from a pattern of a contact hole in the 1st protecting film directly covering a polycryst. Si film over the TFT, so that a short-circuit between lines and a breaking of the lines because of a level difference of film layers. Thus, an occurrence of failure because of the short-circuit between lines is inhibited, and failure in the lines is reduced by reducing the breaking of the source line and/or the drain line.

IT **12033-89-5**, Silicon nitride (Si3N4), uses
RL: DEV (Device component use); USES (Uses)
(insulating film; Active **matrix liq.** **crystal** display device)

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(protecting film; Active **matrix liq.** **crystal** display device)

L33 ANSWER 46 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:285217 HCAPLUS
DN 120:285217
TI Thin-film transistor and **liquid-crystal** display device using same
IN Ogawa, Kazuhiro
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 05181158	A2	19930723	JP 1991-345793	19911227
PRAI JP 1991-345793		19911227		

AB The thin-film transistor comprises, on an insulating substrate, a **gate electrode**, a gate insulating film, a **source electrode**, a **drain electrode**, a high impurity-concn. layer, and a thin-film semiconductor layer in the order. Preferably, the gate insulating film has a 2-layer structure, consisting of a Si oxide film on the **gate electrode** and a Si nitride film.

IT **7631-86-9**, Silicon oxide, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(thin-film transistor contg., for **liq.-crystal** display device)

L33 ANSWER 47 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:257574 HCAPLUS
DN 120:257574
TI **Liquid-crystal** display devices and manufacture thereof
IN Nakatani, Norio; Enomoto, Noboru
PA Sanyo Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 05297409 A2 19931112 JP 1992-104642 19920423
PRAI JP 1992-104642 19920423
AB The manufg. process comprises the steps of forming a gate array and a gate circuit using an anodized Al on a soft glass substrate; forming a SiO2 layer having contact holes; forming (1) a transparent display-electrode array; forming a thin-film transistor (TFT) array comprising (2) a SiNx, (3) an undoped a-Si active, and (4) an n+ a-Si source/drain layer; forming a **source-electrode** array interconnecting (1) and (4); and forming a **drain-electrode** array and a drain circuit linking (4)'s. The process is suited for manufg. large-area display devices.
IT **12033-89-5**, Silicon nitride, uses
RL: USES (Uses)
(TFT active **matrix** from, in **liq.-crystal** display devices)
IT **7631-86-9**, Silicon oxide (SiO2), uses
RL: USES (Uses)
(TFT active **matrix** from, in **liq.-crystal** display devices, manuf. of)

L33 ANSWER 48 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:42061 HCAPLUS
DN 120:42061
TI Active-**matrix** substrate for **liquid-crystal** display device
IN Okumura, Fujio
PA NEC Corp., Japan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5191453	A	19930302	US 1990-570382	19900821
	JP 03080226	A2	19910405	JP 1989-217913	19890823
	JP 2508851	B2	19960619		
	US 5300449	A	19940405	US 1992-963387	19921016
PRAI	JP 1989-217913		19890823		
	US 1990-570382		19900821		

AB An active-**matrix** substrate for a **liq.-crystal** display device comprises a substrate, a plurality of **pixel electrodes** formed on the substrate in a **matrix** form, each of the **pixel electrodes** having a 1st Si thin film and a metal silicide film formed on the 1st Si thin film, and a plurality of thin-film transistors formed on the substrate and connected to the **pixel electrodes**, resp., each of the thin-film transistors having a 2nd Si thin film continuous with the 1st Si thin film, a **gate electrode** formed on one of the upper surface and the lower surface of a portion of the 2nd thin film, and source and drain regions formed at both sides of the **gate electrode**, the **source** and drain regions being connected to the portion of the 2nd thin film and one of the source and drain regions being elec. connected to the **pixel electrodes**.
IT **7631-86-9**, Silicon dioxide, uses **12033-89-5**, Silicon nitride, uses
RL: USES (Uses)
(substrates contg., for active-**matrix liq.-crystal** display devices)

L33 ANSWER 49 OF 52 HCAPLUS COPYRIGHT 2003 ACS

AN 1993:550472 HCAPLUS
DN 119:150472
TI Active-**matrix liquid-crystal** display device
IN Kobayashi, Kazuhiro; Murai, Hiroyuki; Hayama, Masahiro
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05011271	A2	19930119	JP 1991-164140	19910704
	JP 2864794	B2	19990308		
	US 5414278	A	19950509	US 1994-231774	19940425
PRAI	JP 1991-164140		19910704		
	US 1992-904272		19920625		

AB This device contains (1) a 1st insulator protective film which covers thin-film transistors and gate interconnections at the intersections of the gate interconnections and source interconnections, (2) capacitor electrodes; (3) capacitor insulator films which cover part of the capacitor electrodes and the gate interconnections at the interconnections; (4) **pixel electrodes** from a transparent elec. conductive film formed on the capacitor insulator films; (5) a 2nd insulator protective film which covers the **pixel electrodes** and the gate interconnections at the intersections; and drain or source interconnections which connect the drains or sources of the thin-film transistors with **pixel electrodes** across the contact holes in the 1st and 2nd protective films. Optionally, the 1st and 2nd protective films are made of, resp., SiO2 and Ta2O5. Short circuiting between **pixel electrodes** (and capacitor **electrodes**), and **source** or gate interconnections can be prevented.
IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride (Si3N4), uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(protective films, for active-**matrix liq.-crystal** display devices)

L33 ANSWER 50 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:91082 HCAPLUS
DN 118:91082
TI Manufacture of active **matrix liquid crystal** display device having gate-insulating film including tantalum oxide in amorphous silicon transistor
IN Nomoto, Tsutomu; Nobori, Masaharu
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04264774	A2	19920921	JP 1991-24591	19910219
PRAI	JP 1991-24591		19910219		

AB The title display having a transparent elec. insulator-supported thin-film transistor array having a transparent electrode, a **gate electrode**, a gate insulating film, an amorphous Si semiconductor layer, a **source-drain electrode**, and a

surface-protecting film is manufd. by a process including the following steps: (1) forming the 1st gate insulating film comprising TaOx, WTaOx, NiTaOx, CoTaOx, RhTaOx, or IrTaOx by anode chem. formation, (2) forming the 2nd gate insulating TaOx film on the 1st layer by plasma chem. vapor deposition (CVD) or sputtering, (3) forming the 3rd gate-insulating SiOx layer on the 2nd layer by plasma CVD or sputtering, and (4) forming the 4th gate-insulating SiNx film on the 3rd layer by plasma CVD or sputtering. The display shows quick response.

IT **11126-22-0**, Silicon oxide **12033-89-5**, Silicon nitride, uses
RL: USES (Uses)
(gate insulating film, for amorphous silicon transistor array, for **liq. crystal** display device)

L33 ANSWER 51 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:561072 HCAPLUS
DN 117:161072
TI Thin-film-transistor active-**matrix liquid-crystal** display device
IN Kobayashi, Keizo
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04012330	A2	19920116	JP 1990-112639	19900430
	JP 2536230	B2	19960918		
PRAI	JP 1990-112639		19900430		

AB The title device comprises a surface protection film, deposited on a back channel produced by **etching** and consisting of a Si oxide film in **contact** with a semiconductive Si film on the back channel, a Si oxynitride film, and a Si nitride film, wherein the Si oxynitride film has a graded compn. transient from the oxide to the nitride film.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: USES (Uses)
(protective films contg., for **liq.-crystal** display devices)

L33 ANSWER 52 OF 52 HCAPLUS COPYRIGHT 2003 ACS
AN 1991:197851 HCAPLUS
DN 114:197851
TI Thin-film transistors for active-**matrix liquid-crystal** display devices
PA Samsung Electronics Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02260661	A2	19901023	JP 1989-339905	19891227
	JP 06044625	B4	19940608		
	KR 133864	B1	19980423	KR 1988-18214	19881231
	KR 133863	B1	19980423	KR 1988-18215	19881231
	US 5060036	A	19911022	US 1989-458324	19891228
PRAI	KR 1988-18214	A	19881231		

KR 1988-18215 A 19881231

AB The title transistor comprises a **gate electrode** insulated with a SiOx insulator layer having a double-layer structure, and amorphous Si layers sandwiching a Si nitride layer on the SiOx layer. Optionally, the Si layer may be doped with P or B. The transistor has a decreased leakage (or short circuiting) between the gate and **source electrodes**, and a low threshold voltage.

IT **12033-89-5**, Silicon nitride, uses and miscellaneous
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(amorphous films, in thin-film transistors for display devices)

IT **11126-22-0**, Silicon oxide
RL: DEV (Device component use); USES (Uses)
(gate insulators, for thin-film transistors for display devices)

L34 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:833264 HCAPLUS
DN 137:343957
TI Fabrication method of in-plane switching mode active **matrix** type **liquid crystal** display device
IN Nishida, Shinichi; Matsumoto, Kimikazu; Hannuki, Takahisa; Itakura, Kunimasa
PA NEC Corporation, Japan
SO U.S. Pat. Appl. Publ., 123 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002159016	A1	20021031	US 2002-81800	20020222
	JP 2002323706	A2	20021108	JP 2001-350620	20011115
PRAI	JP 2001-48473	A	20010223		
	JP 2001-350620	A	20011115		

AB An in-plane switching (IPS) mode active **matrix** type **liq**. **crystal** display device includes a first substrate, a second substrate located opposing the first substrate, and a **liq**. **crystal** layer sandwiched between the first and second substrates. The first substrate includes a thin film transistor, a **pixel electrode** each assocd. to a pixel to be driven, a common electrode to which a ref. voltage is applied, data lines, a scanning line, and common electrode lines. Mol. axes of **liq**. **crystal** are rotated in a plane parallel with the first substrate by an elec. field substantially parallel with a plane of the first substrate to display certain images. The common electrode is composed of transparent material, and are formed on a layer located closer to the **liq**. **crystal** layer than the data lines. The common electrode entirely overlaps the data lines except an area where the data lines are located in the vicinity of the scanning line. The **liq**. **crystal** display device further includes a light-impermeable layer in an area where the common electrode entirely overlaps the data lines. The light-impermeable layer is comprised of a black **matrix** layer having a width smaller than a width of the common electrode. The object of the present invention is to provide an IPS mode **liq**. **crystal** display device which is capable of preventing occurrence of vertical cross-talk without redn. in an aperture ratio.

L34 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:566705 HCAPLUS
DN 135:129671
TI Active **matrix** substrate, method for fabricating the substrate, and **liquid crystal** display device
IN Izumi, Yoshihiro; Chikama, Yoshimasa; Ochi, Hisao
PA Japan
SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001010566	A1	20010802	US 2001-768725	20010124
	JP 2001282139	A2	20011012	JP 2000-307927	20001006
PRAI	JP 2000-18750	A	20000127		
	JP 2000-307927	A	20001006		

AB **Pixel electrode** fabricating processes are remarkably reduced. A **pixel electrode** is formed without using any vacuum film forming app. by employing a sol-gel material and coating an insulating substrate with the sol-gel material by a spin-coating method or a dipping method, and this allows the fabricating processes to be reduced. During this course, by forming the **pixel electrode** before the formation of a scanning electrode , signal wiring lines and a TFT , the electrode wiring and the TFT suffer no thermal damage even if they have a heat resistance temp. of .apprx.350.degree.. also, by using a sol-gel material having photosensitivity, patterning processes are reduced by the elimination of the photoresist patterning process and the etching process. An investment for the equipment of a fabricating app. can thus be reduced to allow the cost redn. of the active **matrix** substrate itself to be achieved.

L34 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:472024 HCAPLUS
DN 131:123914
TI Semiconductor device and its manufacture
IN Nakazawa, Misako
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11202368	A2	19990730	JP 1998-18050	19980114
	US 2002000613	A1	20020103	US 1998-197767	19981123
PRAI	JP 1997-344350	A	19971127		
	JP 1998-18050	A	19980114		

AB The device having double elec. conductive layer sandwiching an elec. insulator layer is elec. connected through an oxide elec. conductor filled on a **contact hole** formed on the insulator layer. An elec. insulator layer is formed on a bottom elec. conductor layer, a **contact-hole** is **opened** through the insulator layer, and an oxide elec. conductive layer is formed by spin coating a soln., e.g., an org. solvent soln. of an ITO org. compd. etc., on the intermediate insulator layer. Then, the oxide conductive layer is annealed and is back-**etched** so that the oxide conductive layer fills only the **contact-hole**. Then, an top elec. conductive layer formed on the insulator layer. The whole surface becomes plane because the oxide conductive layer fills the **contact-hole** completely. The manuf. is applied to an AMLCD (active **matrix liq. crystal** display), for example.

L34 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:617887 HCAPLUS
DN 127:302068
TI LDD thin-film transistors, active **matrix** arrays for **liquid crystal** display devices, and fabrication thereof
IN Furuta, Mamoru; Tsutsu, Hiroshi; Kawamura, Tetsuya
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 09246558 A2 19970919 JP 1996-53553 19960311
PRAI JP 1996-53553 19960311
AB The title fabrication of TFTs involves forming a **silica** film as a buffer layer on a glass substrate, depositing a polycryst. Si thin-film and patterning to give an active layer, forming a **silica** gate insulator film and a Al-10% Zr alloy **gate electrode** on the active polycryst. Si layer, forming a SiNx or TaOx film as a doping mask over the **gate electrode** and a lightly-doped region of the thin-film transistor, and subsequently doping with P over the mask. The process gives a LDD structure without sequential doping processes and provides the TFTs with decreased OFF current.

L34 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:672581 HCAPLUS
DN 125:312613
TI Thin film transistor (TFT) and active **matrix liquid crystal** display using same for good contrast and image stability
IN Yamaguchi, Takehisa
PA Mitsubishi Electric Corp, Japan; Asahi Glass Co Ltd
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08220558	A2	19960830	JP 1995-21541	19950209
PRAI JP 1995-21541		19950209		

AB The title TFT has on a transparent insulative substrate a light-shielding film, an insulative film, a gate protection film, an .alpha.-Si i layer, a channel protection film, an .alpha.-**Si n+** layer, a **source electrode**, and a pair of **drain electrodes**. The display has a **liq. crystal** between a TFT-bearing array substrate and an opposite substrate and a has a back light for irradiating from the above array substrate side.

L34 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:209978 HCAPLUS
DN 124:246620
TI **Matrix** type **liquid crystal** display apparatus and its manufacture
IN Suzuki, Shoji
PA Mitsubishi Electric Corp, Japan; Asahi Glass Co Ltd
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08029808	A2	19960202	JP 1994-166879	19940719
PRAI JP 1994-166879		19940719		

AB The title app. contains a Si ladder polymer film(s) on transparent areas of a substrate(s). The title app. comprises a Si ladder polymer-contg. insulator interlayer between a **source-drain electrode** and a **gate electrode**.

L34 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:986188 HCAPLUS
DN 124:18543
TI Active **matrix** thin film transistor **liquid**

crystal display and its manufacture
IN Matsuda, Yoji
PA Sanyo Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07270821	A2	19951020	JP 1994-57803	19940328
PRAI JP 1994-57803		19940328		

AB In the title display comprising TFT, a **liq. crystal** cell, and an auxiliary capacity, the elec. capacity is formed between the counter electrode of the auxiliary capacity and the **pixel electrode** of the TFT.

L34 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:623399 HCAPLUS
DN 123:23973
TI Thin-film transistor and display using the transistor
IN Miura, Yasunori; Shibusawa, Makoto; Sugahara, Atsushi; Seiki, Masahiro
PA Kabushiki Kaisha Toshiba, Japan
SO PCT Int. Appl., 52 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9425990	A1	19941110	WO 1994-JP658	19940421
W: US				
RW: DE, FR, GB				
JP 07094753	A2	19950407	JP 1994-81815	19940420
EP 647971	A1	19950412	EP 1994-913790	19940421
EP 647971	B1	19990714		
R: DE, FR, GB				
EP 813251	A2	19971217	EP 1997-115043	19940421
EP 813251	A3	19980114		
R: DE, FR, GB				
US 5563432	A	19961008	US 1994-360743	19941223
PRAI JP 1993-96328		19930423		
JP 1994-81815		19940420		
EP 1994-913790		19940421		
WO 1994-JP658		19940421		

AB A thin-film transistor suited for use in an active-**matrix** **liq. crystal** display panel, reduces a photoelectron leak current, thereby achieving a high ON/OFF current ratio.

L34 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:712216 HCAPLUS
DN 121:312216
TI MIM **liquid crystal** panel
IN Yazawa, Satoru
PA Seiko Epson Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 06130421	A2	19940513	JP 1992-276104	19921014
PRAI	JP 1992-276104		19921014		

AB In the title **matrix liq. crystal** panel having switching devices on one side of a substrate, the switching devices connected to each **pixel electrodes** comprises .gtoreq.2 MIM devices having reverse connections, and the switching devices, date lines transmitting signals to the switching devices and the **pixel electrodes** are coated with a passivation film having thickness .gtoreq.1500 .ANG.. The **liq. crystal** panel showed no after image and improved humidity-resistant characteristics.

L34 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:49411 HCAPLUS
DN 118:49411
TI active-**matrix liquid-crystal** display device
IN Nishimura, Kenichi; Tanaka, Hirohisa; Hishida, Tadanori
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04163528	A2	19920609	JP 1990-292719	19901029
	JP 2963529	B2	19991018		
	JP 11326941	A2	19991126	JP 1999-117476	19901029
PRAI	JP 1990-292719		19901029		

AB The title device comprises a transparent insulator base, a thin-film transistor array, a **multilayer** transparent **insulator** film consisting of alternating org. and inorg. thin films, and a **pixel electrode** array.

L34 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:662384 HCAPLUS
DN 117:262384
TI Study of the Vth shift of the thin-film transistor by the bias temperature stress test
AU Fujimoto, Yukinobu
CS IBM Japan, Yamato, 242, Japan
SO IBM Journal of Research and Development (1992), 36(1), 76-82
CODEN: IBMJAE; ISSN: 0018-8646
DT Journal
LA English
AB Amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as the switching device in the active-**matrix** addressing of **liq. crystal** displays. One concern is the potential instability problems assocd. with the threshold voltage (Vth) shifts to higher values after prolonged operating times. The reason for this Vth shift has been widely discussed, and two models accounting for it have been suggested. One model explains the shifts by the trapping of electrons in the insulator, the other model by the creation of the metastable states at the a-Si:H/SiNx interface. The TFT insulator has the rather complicated structure of an anodic oxide film, SiOx, SiNx sequentially stacked over the **gate electrode**, which makes it difficult to sep. the contribution of each layer. Expts. show that the anodic oxide film makes no contribution to the Vth shift, and it makes little difference to the Vth shift whether the next insulator is SiNx or SiOx. The mechanisms of the latter fact are discussed.